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Research Article

Compact Two-Stage CMOS Operational Amplifier with Enhanced Gain and Bandwidth via Cascode and Negative Capacitance Techniques

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Abstract: In this research, a two-stage CMOS amplifier has been developed, characterized by high gain, extensive frequency bandwidth, and a compact chip area. The design incorporates a negative capacitor unit, a flipped voltage follower, a cascode configuration in the first stage, and a small MOSFET-based capacitor. The use of negative capacitance effectively diminishes the parasitic capacitance from the previous stage, resulting in a notable improvement in gain bandwidth. The flipped voltage follower functions as a voltage buffer within the circuit and utilizes pole-zero cancellation techniques to improve frequency bandwidth. This design enhances the amplifier's performance by effectively managing stability and response characteristics. Additionally, modifications to the input stage of the operational amplifier through a cascode structure yield a significantly high-gain amplifier. The first stage's cascode arrangement for the MOSFET drivers, along with an active load that has high output resistance, accounts for the majority of the circuit's gain. By eliminating passive capacitors and substituting them with small MOSFET-based capacitors, the proposed design effectively reduces chip area while boosting gain bandwidth. The design and simulation processes were carried out using Cadence IC Design Virtuoso software based on standard TSMC 0.18 µm CMOS technology. The results indicate that the amplifier achieves a DC gain of 80 dB, a bandwidth of 1.3 GHz, and a phase margin of 84 degrees.

Keywords: Two-stage CMOS amplifier, Flipped voltage follower, Cascode structure, Negative capacitance MOSCAP.

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1. INTRODUCTION

The operational amplifier (Op-amp) serves as a fundamental component in nearly all signal processing systems, typically employed within a feedback loop to ensure stable and predictable gain with minimal noise. Its differential and mathematical operational capabilities have facilitated analog computations and automation within mixed-signal environments. However, Op-amps that utilize bipolar junction transistors (BJTs) tend to consume more power 1, rendering them unsuitable for many modern application-specific integrated circuits (ASICs) [1]. In contrast, Op-amps based on metal-oxide-semiconductor field-effect transistors (MOSFETs) are becoming increasingly significant in contemporary signal processing architectures due to their potential for low-power operation. Nevertheless, their performance is often hindered by a lower transconductance to drain current ratio (gm/Id < 28) compared to the gm/Id ratio of approximately 40 for BJTs, along with issues such as poor matching and low output impedance in the strong inversion region [2, 3].

The compensation techniques employed in operational amplifiers often require considerable chip area and involve more intricate designs compared to the traditional dominant pole approach (pole splitting) commonly used in classical op-amp architectures [4,5]. Historically, the Miller effect has been utilized to create a large capacitance at the output of the high-gain differential first stage. However, a feed-forward path is also present, introducing a positive zero that affects phase characteristics similarly to a pole, which can reduce the phase margin. Typically, a nulling resistor is added in series with the compensating capacitor to adjust the location of this zero, which further increases chip area usage [6-9].

Compensation techniques utilizing a current buffer, specifically through a common gate transistor, are highly effective in enhancing the gain-bandwidth product and power supply rejection ratio (PSRR) performance. These methods allow for smaller minimum allowable values of the compensation capacitor (CC), which provides greater flexibility in balancing noise performance against power consumption. A reduced CC facilitates improved design options, enabling engineers to optimize the operational amplifier's performance while maintaining low power usage [10].

In Miller and current buffer compensation techniques, the compensation capacitor usually adds a load to the output node. However, when a voltage buffer is incorporated into the feedback loop, the compensation capacitor reduces this loading effect on the output node. Additionally, the low impedance at the output node enhances effective feedback. This compensation approach exhibits high accuracy, as it primarily depends on the matching tolerances between transconductance and capacitance. Furthermore, compensation techniques that utilize a nulling resistor alongside a voltage buffer yield the same compensation capacitor and maintain an equivalent gain-bandwidth product [11-13]. Practical voltage buffers can be created using a common-drain (CD) transistor. This paper introduces a proposed compensation technique that employs a variant of the flipped voltage follower (FVF). In many applications, FVFs exhibit better performance than traditional CD configurations due to their remarkably low output impedance. The FVF cell enables the circuit to attain a wide range of transconductance while preserving good linearity throughout the input range. This capability is crucial for applications requiring precise control over frequency response and signal processing. This capability is essential for maintaining consistent performance across various operating conditions [14, 15]. The schematic of a PMOS version of the FVF is illustrated in Fig. 1. The FVF consists of a PMOS input transistor (M_{FVF}), a transistor (M_2) with shunt feedback. Also, the proposed compensation technique involves a transistor (M_{bias}) that is used to create the bias current [14]. This configuration is essential for ensuring stable operation of the circuit. While the FVF is capable of sourcing high currents, its ability to sink current is somewhat limited. The internal feedback loop plays a crucial role in reducing the output impedance $1/gm_{FVF}$ of the control transistor by the loop gain gm_2r_{oFVF}. Consequently, the output impedance of the FVF is given by:

$$R_{out} = \frac{1}{g_{mFVF}(g_{m2}r_{oFVF})} \quad (1)$$

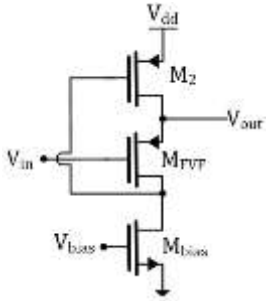


Fig. 1: Schematic representation of the Flipped Voltage Follower (FVF).

As shown in Fig. 1, which depicts the FVF. This circuit can achieve a high slew rate while maintaining low quiescent current consumption. Additionally, a MOS capacitor (MOSCAP)-based frequency compensation method minimizes die area usage, effectively eliminating passive elements that occupy space on the die. Consequently, the die area can be fully allocated to MOSFETs. In high-frequency applications, where parasitic capacitance can adversely affect performance, the incorporation of negative capacitance significantly reduces it for the preceding stage. This approach is essential for maintaining signal integrity and enhancing the overall efficiency of the circuit. The discussed paper employs a MOSCAP configured as a negative capacitance in conjunction with a voltage buffer, enhancing both the slew rate and the unity gain frequency of multistage CMOS circuits. In this setup, the first stage is designed with active negative capacitance, which plays a crucial role in optimizing circuit performance. This innovative use of negative capacitance effectively reduces the adverse effects of parasitic capacitances through partial cancellation, leading to significant improvements in both unity gain frequency and phase response. The equation for bandwidth (BW) of an operational amplifier driving a parallel combination of load resistance R1 and parasitic capacitance C_1 is given by:

$$BW = \frac{1}{2\,\pi\,C_1\,R_1} \quad (2)$$

To enhance bandwidth, reducing the value of C_1 through techniques such as negative capacitance is effective. Negative capacitance can counteract the effects of parasitic capacitance, effectively lowering the total capacitance seen by the amplifier and allowing for a higher bandwidth.

The practical circuit described utilizes a MOSCAP as a negative capacitance, replacing the traditional negative capacitor (C_N) to enhance performance metrics in multistage CMOS circuits. In this configuration, the components R_2 and C_2 are indicative of the output resistance and parasitic capacitance, respectively, which significantly affect the frequency response of the circuit [15].

The design of the proposed amplifier focuses on effectively managing both the load capacitance associated with the amplifying stage and the input capacitance related to the Negative Capacitance Generator (NCG) circuit. This dual consideration is crucial for ensuring optimal performance and stability of the amplifier in various applications. The MOSCAP functions as a negative capacitor by connecting the amplifier's output to the gain A, effectively creating a negative capacitance. By incorporating the NCG circuit into the amplifier's output node, the bandwidth is extended and can be expressed mathematically as:

$$C_N = C_N(1 - A_V) \quad (3)$$

The total capacitance is given by:

$$C_{tot} = C_N \,||(C_1 + C_2) \quad (4)$$

The bandwidth P can be calculated as:

$$P = \frac{1}{C_{tot}\, R} \tag{5}$$

The introduction of a NCG into a circuit significantly influences its frequency response by creating new poles and zeros. To optimize the performance of the NCG, it is essential to ensure that the magnitude of the zero is much greater than that of the poles. This condition allows the zero to be effectively neglected, which enhances the bandwidth of the circuit [16, 17].

This paper is organized as follows: Section 2 of the discussion focuses on the transfer function, the determination of pole-zero characteristics, and the criteria for stability in operational amplifier circuits. The results in this section clearly demonstrate that the proposed compensation technique improves phase margin and extends bandwidth, as elaborated in Section 3. Section 4 outlines widely accepted figures of merit (FOM$_s$) used to compare the performance of different designs. In this section, we delve into the performance of the proposed circuit in comparison to existing state-of-the-art designs. The analysis focuses on key performance metrics such as gain, bandwidth, slow rate, and input/output characteristics. Finally, Section 5 concludes with a summary of the proposed methodology and suggests directions for future research [18, 19].

2. PROPOSED TWO-STAGE AMPLIFIER

The proposed two-stage amplifier is meticulously designed to achieve an adequate GBW and a high phase margin, which are essential for efficient performance in various applications. The circuit extends the unity gain frequency and enhances operational speed while satisfying stability requirements.

The proposed circuit employs three frequency compensation techniques: the FVF, MOSCAP, and NCG block. The block diagram of this configuration is illustrated in Fig. 3, while its transistor-level implementation is detailed in Fig. 4. The proposed two-stage amplifier, as illustrated in Fig. 3, consists of two gain stages connected in series, with a Feedback Voltage (FVF) block and a MOSCAP serving as the Cc placed between nodes A and B. This configuration is critical for ensuring stability and enhancing performance. The FVF block operates as a voltage buffer, implemented using transistors M_{10}–M_{12}, while the MOSCAP serves as the *Cc*.

This configuration effectively enhances both linearity and speed within the circuit. The proposed circuit utilizes a MOSCAP not only as the compensation capacitor but also to enhance the phase margin of the amplifier. Additionally, a feedback MOSCAP, denoted as C_N, plays a crucial role in bandwidth enhancement. The inclusion of the MOSCAP allows for the elimination of passive elements from the circuit, thereby reducing die area occupation.

Furthermore, the input stage of the proposed operational amplifier has been modified using a cascode structure, resulting in a very high-gain amplifier. The first stage employs a cascode structure for the MOSFET drivers and

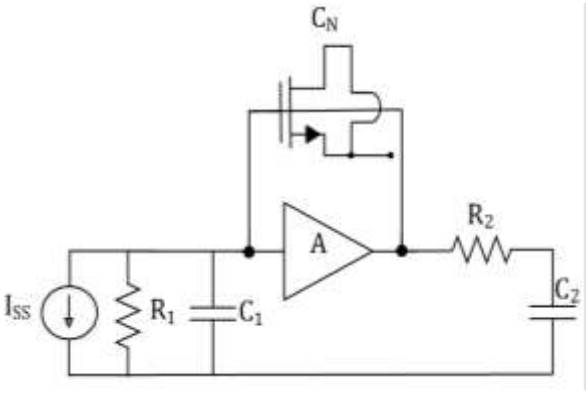


Fig. 2: Generation of negative capacitance utilizing a MOSCAP.

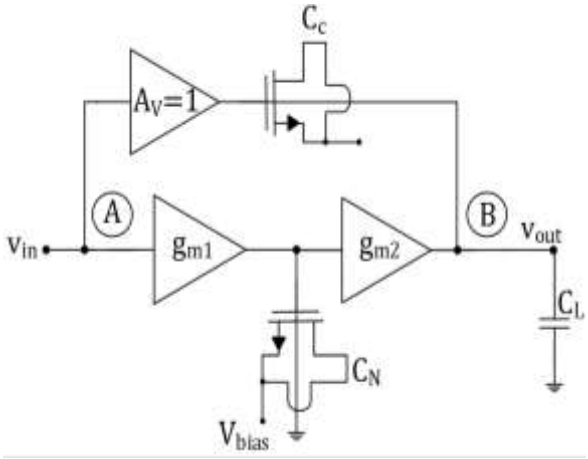


Fig. 3: Schematic representation of the proposed circuit's block diagram.

an active load with high output resistance, which contributes significantly to the overall gain of the circuit. The NCG circuit also plays a crucial role by maximizing the zero in the circuit's transfer function, leading to an increase in gain-bandwidth product (GBW). The output stage of the proposed amplifier is configured as a common source amplifier, utilizing and NMOS transistor (M_{13}) and a PMOS transistor (M_{14}). This configuration is widely recognized for its effectiveness in providing high gain and good linearity in signal amplification. The equivalent circuit for small signal analysis of the proposed compensation technique is illustrated in Fig. 5. In this configuration, the input stage is characterized by an output resistance r_{o1}, output capacitance C_1 and transconductance g_{m1}. The small signal model facilitates the evaluation of the amplifier's performance by allowing for linear analysis around a specific operating point. The first stage is loaded with a NCG, which produces a negative capacitance that effectively mitigates the effects of parasitic capacitance from the first stage. The final stage of the amplifier is configured as a common source amplifier, which includes an output resistance r_{o2}, total equivalent load capacitance C_L and transconductance g_{m2}.

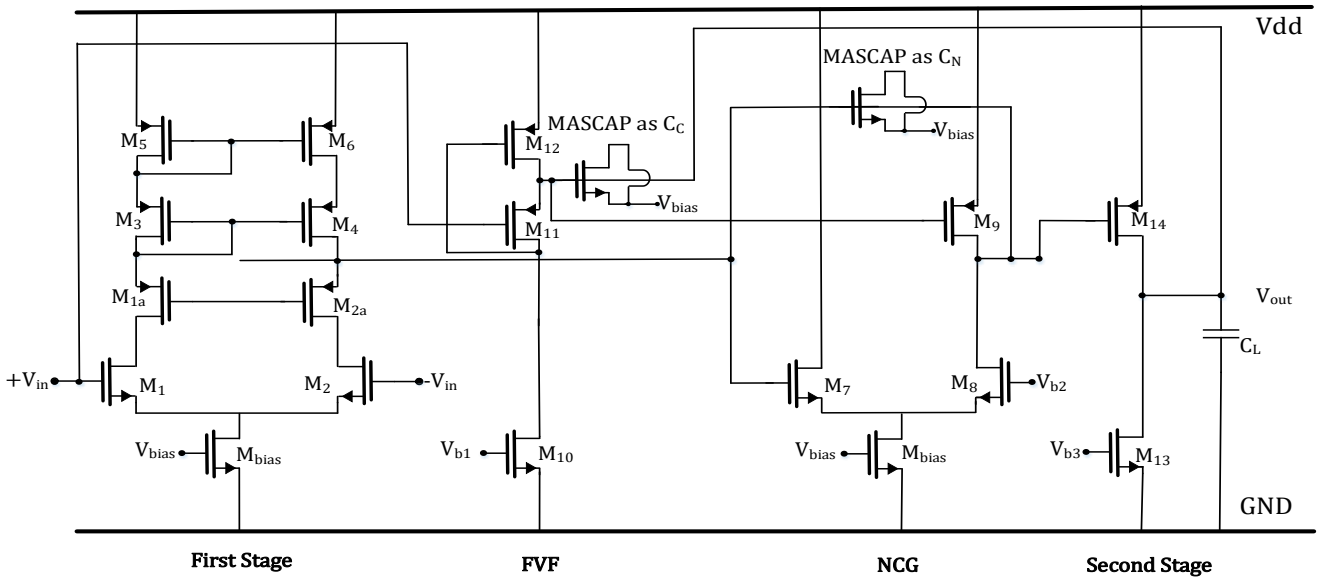


Fig. 4: Implementation of the proposed compensation technique at the transistor level.

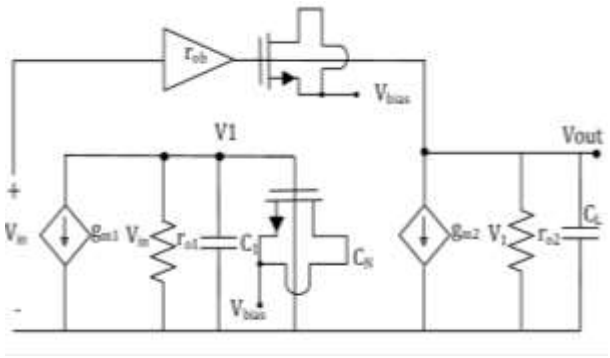


Fig. 5: Equivalent circuit for small signal analysis of the proposed compensation technique.

This configuration is known for its ability to provide significant voltage gain and is widely used in analog circuit designs. The voltage buffer, represented by the FVF cell, connects nodes A and B, with its output impedance denoted as r_{ob}. The FVF is a specialized buffer circuit known for its low-power and low-voltage operation, making it particularly suitable for modern analog and mixed-signal applications.

The small-signal transfer function of compact two-stage CMOS operational amplifier can be expressed as a second-order equation, which is crucial for analyzing the amplifier's frequency response and stability. This transfer function typically takes the form:

$$A_V = \frac{(C_C r_{o1} + C_C r_{ob})s}{\left((C_1 + C_C)r_{o1} + (C_C + C_L)r_{ob} + C_N\right)S^2} \quad (6)$$

$$\frac{+g_{m1}g_{m2}}{+\left((C_1 + C_C)(C_C + C_L)r_{o1}r_{ob}\right)S + \left(\frac{1}{(r_{o1}r_{ob})}\right)}$$

The transfer function of the proposed compact two-stage CMOS operational amplifier can be characterized by its poles, zeros, GBW, and phase margin (PM). The relevant equations for these parameters are defined as follows:

The first pole is defined as:

$$P_1 = \frac{1}{\left((C_1 + C_C)r_{o1} + (C_C + C_L)r_{ob} + C_N\right)} \quad (7)$$

The second pole is given by:

$$P_2 = \frac{1}{\left((C_1 + C_C)(C_C + C_L)r_{o1}r_{ob}\right)} \quad (8)$$

The zero is defined as:

$$\Im = (C_C r_{o1} + C_C r_{ob}) \quad (9)$$

The gain-bandwidth product is calculated as:

$$GBW = \frac{g_{m1}g_{m2}r_{o1}r_{ob}}{\left((C_1 + C_C)r_{o1} + (C_C + C_L)r_{ob} + C_N\right)} \quad (10)$$

The phase margin is determined by:

$$PM = 180 - tan^{-1}\left(\frac{GBW}{P_1}\right) - tan^{-1}\left(\frac{GBW}{P_2}\right) \quad (11)$$

The effective capacitance at the output of the first stage, represented as $C_1+C_N(1-A)$, is indeed reduced, which plays a significant role in improving the performance of the amplifier. Additionally, the small output impedance rob of the FVF contributes positively to frequency compensation. As a result, the

poles defined in (7) and (8) are positioned farther from the unity gain frequency, thereby extending the overall bandwidth of the amplifier.

3. Simulation Results

The proposed compact two-stage CMOS operational amplifier presented here introduces a method for frequency compensation in a two-stage CMOS circuit utilizing negative capacitance through a MOSCAP and the FVF. This approach effectively enhances the performance of the amplifier by addressing stability issues and improving bandwidth. Additionally, the implementation of a cascode structure in the first stage significantly enhances the amplifier's gain. Implementation of the proposed compensation technique at the transistor level, illustrated in Fig. 4, has been simulated using the Cadence Virtuoso 6.17 simulation tool with TSMC CMOS 0.18 µm process parameters. The maximum bias current in the circuit is 1.22 mA and supply voltage is set to 1.8 V. All transistors are working in saturation mode and their aspect ratios and other circuit component values are mentioned in Tables 1 and 2, respectively. The slew rate of proposed circuit is very high as the output voltage of the given circuit changes rapidly with respect to time. The simulated transient response with a 1 pF load for rising and falling edge is shown in Fig. 6 and slew rate (±) measured is 155 V/µS. The overshoot and 1 % settling time (average) of the circuit is calculated as 0.860 µV and 1.72 µS respectively. The average slew rate is 155 V/µS which is very high as compared to other reported techniques [16, 21-23].

The AC analysis of the proposed amplifier was conducted for various values of load capacitance (C_L), and the results are illustrated in Fig. 7. This simulation is essential for analyzing how different load capacitances affect the amplifier's frequency response, stability, and overall performance. The performance of the amplifier remains robust across different load capacitor values. Specifically, the amplifier achieves GBW of 1.45 MHz, 1.41 MHz, and 7.48 MHz with corresponding PM of 81°, 84°, and 107° for load capacitances of 0.1 pF, 1 pF, and 10 pF, respectively.

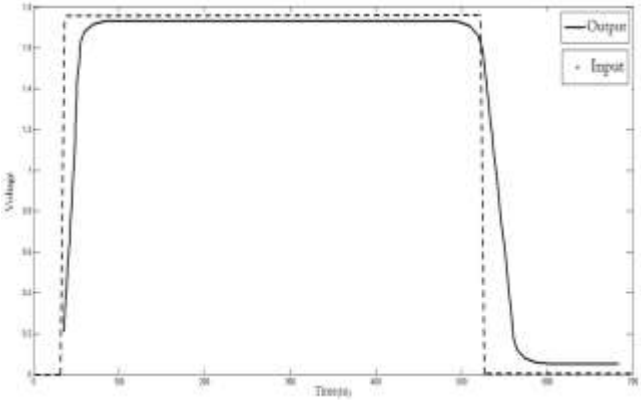


Fig. 6: The step response of the proposed amplifier with a load capacitance of 1 pF.

Table 1: MOSFETs dimensions.

MOSFET	$W(\mu m)/L(\mu m)$	MOSFET	$W(\mu m)/L(\mu m)$
M_1 and M_2	56/180	M_{10}	68/180
M_3 and M_4	70/180	M_{11} and M_{12}	40/180
M_5 and M_6	77/180	M_{13}	20/180
M_7 and M_8	73/180	M_{14}	40/180
M_9 and M_{99}	75/180	M_{1a} and M_{2a}	70/180

Table 2: Circuit parameters and corresponding numerical values.

Parameter	Simulated results	Unit
Gain	80	dB
Gainbandwidth product	1.4	GHz
Current Total	1220	µA
Supply Voltage	1.8	V
Technology	18	µm
Phase margin	84	(°)
Slew rate	155	(V/µS)
CL(pF)	1	Pf
Cc(pF)	0.001	Pf
FOM1	866	-
FOM2	93	-
Power	1.620	mW

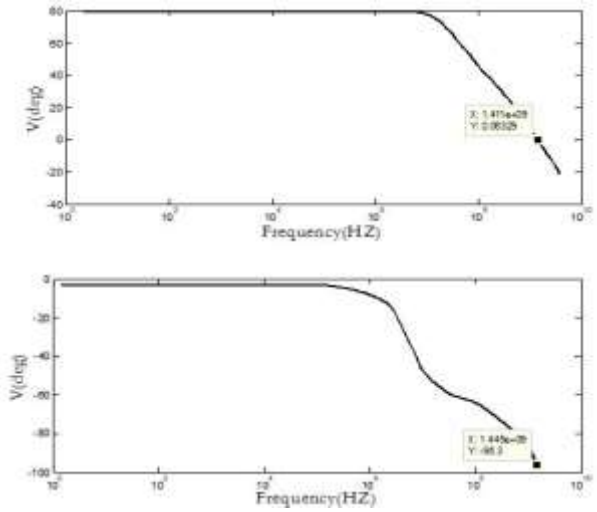


Fig. 7: Gain and phase characteristics of the proposed circuit with a load capacitance of C_L=0.1 pf.

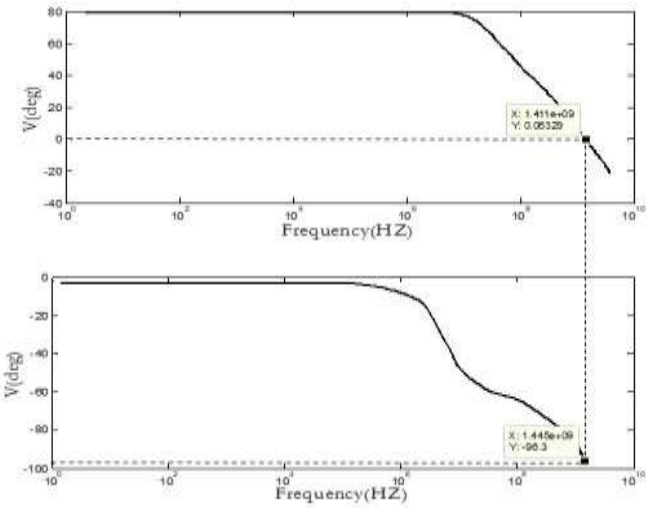


Fig. 8: Gain and phase characteristics of the proposed circuit with a load capacitance of C_L=1 pf.

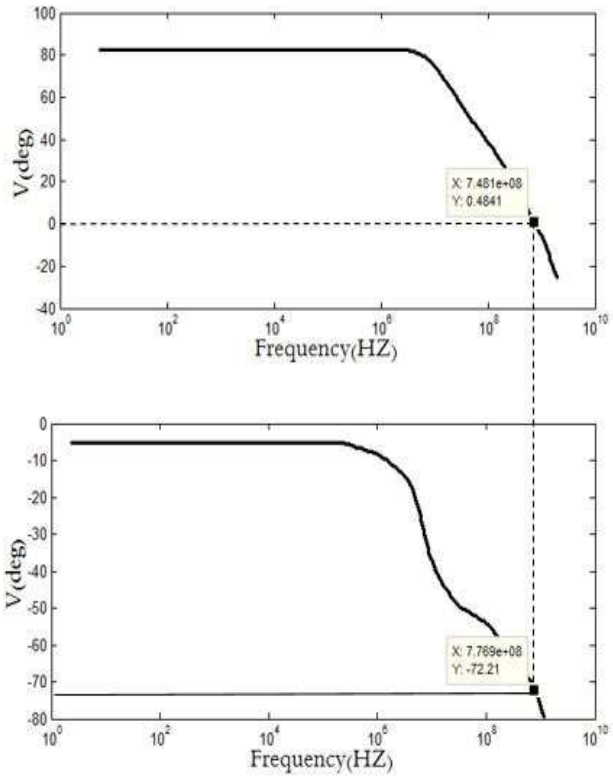


Fig. 9: Gain and phase characteristics of the proposed circuit with a load capacitance of C_L=10 pf.

The output voltage swing of the proposed circuit (Fig. 10), which ranges from 0.2 V to 1.50 V, demonstrates an improvement over the first stage cascode circuit. This enhancement in output voltage swing can be attributed to several factors: In the proposed circuit, two MOSCAPs are utilized in place of passive capacitors for negative capacitance and compensation purposes. This design choice leads to a significant reduction in chip area, as demonstrated by the equivalent circuit analysis. The calculated chip area using MOSCAPs is 3669 µm², compared to 4527 µm² when using traditional passive capacitors.

4. DISCUSSION

The proposed compensation technique has been evaluated against established topologies using two key FOM: FOMS for small-signal behavior and FOML for large-signal behavior. These figures of merit are defined as follows:

FOMS (Small Signal Behavior):

$$FOM_S = (GBW * C_L)/Iss \quad (12)$$

FOML (Large Signal Behavior):

$$FOM_L = (GBWdemonstrates * SLOW * C_L)/Iss \quad (13)$$

The proposed circuit for bandwidth extension a significant improvement in performance compared to existing techniques, as summarized in Table 3. While it requires a considerable number of transistors, it achieves an optimal

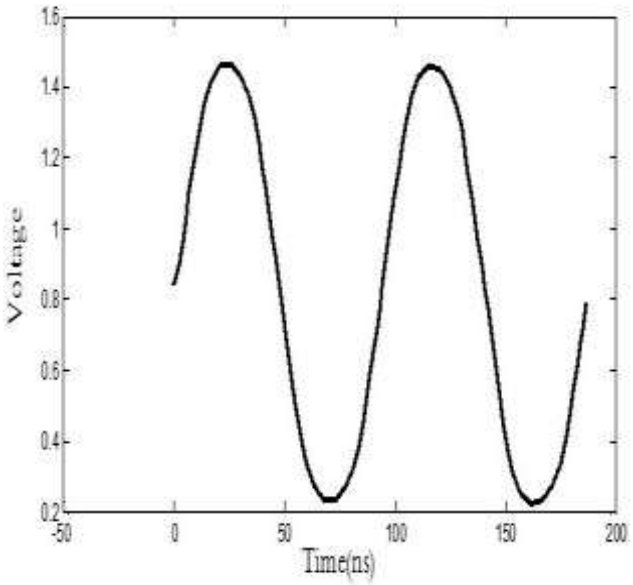
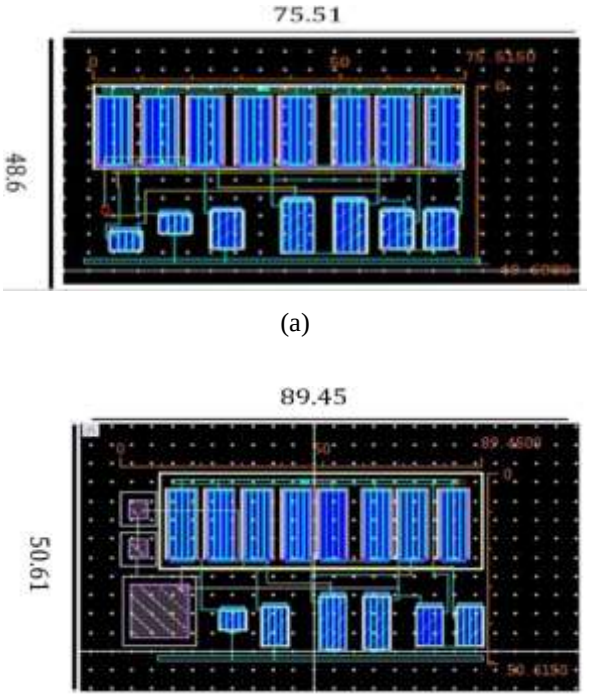


Fig. 10: Output voltage swing of proposed circuit.



(a)

(b)

Fig. 11: Layout of proposed circuit (a) with MOSCAP (b) without MOSCAP.

combination of GBW, transconductance (GM), and PM. The high slew rate and elevated values of PM and GM indicate enhanced stability. Additionally, the calculated FOM values show substantial improvements over previously reported methods [16, 21-23]. Notably, the load capacitance utilized in the proposed circuit does not influence the FOMs, which is a crucial advantage. The cascode op-amp configuration employed contributes to a higher DC gain. Overall, this circuit is characterized by its simplicity and capability to operate effectively at very high frequencies.

Table 3: Performance comparison whit some other research.

	DC gain (dB)	Load (pF)	Power (mW)	GBW (GHz)	Compensation Capacitor(pF)	Slew rate (V/µS)	P.M (°)	FOM1	FOM2
[21]	58.59	15	--	0.81	0.001	5.3	60.7	160	--
[22]	67	30	2.588	0.29	3.5	13.8	51	351	45
[23]	54	2.5	1.9	0.55	0.009	17.33	94.9	--	--
[16]	61	1	1.620	1.2	5.6	148	73	740	90
Proposed circuit	80	1	1.740	1.4	0.001	155	84	864	93

5. Conclusion

In this research, a two-stage CMOS amplifier has been designed with the goals of achieving high DC gain, wide frequency bandwidth, and a compact chip area. To enhance the amplifier's gain, a cascode configuration was implemented in the first stage. This structure effectively increases the DC gain while maintaining stability. A compensation capacitor was utilized to improve the frequency response of the amplifier. The FVF serves as a practical voltage buffer in this compensation technique, benefiting from its very low output impedance, which enhances overall performance. The incorporation of negative capacitance reduces the parasitic capacitance from the preceding stage, leading to significant improvements in GBW. The addition of a NCG introduces new poles and zeros at high frequencies, optimizing bandwidth by maximizing the zero while ensuring it is considerably larger than the poles. The use of MOSCAPs for frequency compensation minimizes die area by eliminating passive components. This allows the die area to be fully allocated to MOSFETs, resulting in a reduced chip area of 3669 µm². Simulations were conducted using Cadence IC Design Virtuoso software with TSMC 0.18 µm CMOS technology. Key performance metrics include: Slew Rate: ±155 V/µs, Overshoot: 0.86 µV, Settling Time: 1.72 µs, GBW values of 1.45 MHz, 1.41 MHz, and 7.48 MHz with corresponding phase margins of 81°, 84°, and 107° for load capacitances of 0.1 pF, 1 pF, and 10 pF, respectively. Output Voltage Swing: Ranges from 0.2 V to 1.40 V. The amplifier's performance was evaluated under varying load capacitance conditions, demonstrating that the load capacitance does not adversely affect the figures of merit.

Credit Authorship Contribution Statement

MohammadMehdi Derakhshannia: Formal analysis, Resources, Software, Visualization, Writing - review & editing. **Mohsen Shakiba:** Conceptualization, Methodology, Project administration, Resources, Software, Supervision. **Maryam Shakiba:** Conceptualization, Investigation, Methodology, Resources, Validation, Writing - original draft, Writing - review & editing**.**

Declaration Of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper. The ethical issues; including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, redundancy has been completely observed by the authors.

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