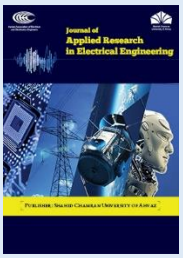
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Research Article

An Algorithm for Determining the Desirability of the Amount of Transient Limiting Reactors in Shunt Capacitor Banks

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Abstract: Capacitor banks are commonly used in power grids for purposes such as power control and power factor correction. Capacitor banks are exposed to high-amplitude and high-frequency currents in circuit breaker switching. Also, if a fault occurs near the substation where the capacitor bank is installed, the energy stored in the capacitor bank at the fault location is discharged. The discharge of this energy causes currents to pass through at a high frequency and in large quantities. These high currents cause damage to the circuit breaker. To prevent these deleterious effects, the use of transient limiting reactor in capacitor banks is recommended. In this paper, an algorithm for determining the desirability of the amount of transient limiting reactors in shunt capacitor banks is designed based on the IEC Std 62271 standard. The algorithm was then developed for use in the electrical industry in the form of a software called Transient Analyzer. In the developed software, the C# programming language is used to develop and implement algorithms and data processing. The software has been tested and debugged using data from 20 regional electricity substations in Khuzestan. The proposed software is highly efficient compared to the conventional simulation method and can be used with simple data entry and fast processing and presentation of results and data analysis in a short time.

Keywords: Inrush currents, Shunt capacitor bank, Transient limiting reactor, Transient analysis software, IEC standard.

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1. INTRODUCTION

1.1. Background

Shunt capacitor banks are used for correction of voltage profile, power factor and elimination of specific harmonics in the power network [1]. Among the essential considerations related to the use of these equipment in the power network are the presence of transient states caused by them. These transient states are 1) the inrush current caused by the transient state of a single capacitor bank connected, 2) the inrush current caused by the back-to-back connected capacitor bank transient state, and 3) the transient current caused by the energy discharge of the capacitor bank in the event of a near external fault. Modes (2) and (3) can be seen in Fig. 1.

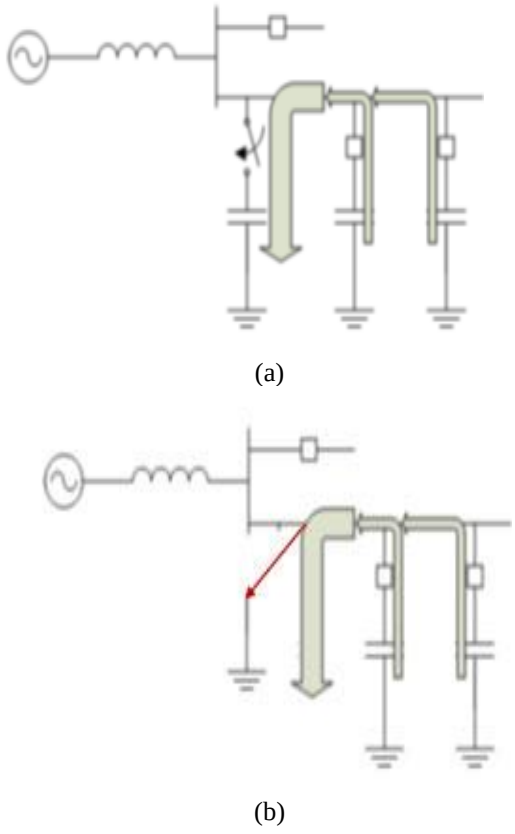
These transient states can have dangerous consequences, such as the failure of circuit breaker connections due to the passage of high-frequency current for single and back-to-back capacitor bank switching and the failure of the circuit breaker to operating properly for the near-fault. To prevent or reduce these transient states, there are various solutions, one of which is the use of transient limiting inductors [2]. This solution is reliable and economical, and the mentioned inductors do not need a short-term maintenance period. The mentioned inductors are installed in series with the capacitor bank to limit transient current. For example, in shunt capacitor banks with a star connection, these inductors are placed between the busbar and the circuit breaker, between the circuit breaker and the capacitor bank or between the capacitor bank and the neutral point in each phase.

1.2. Related Research

In [2], the issue of using transient limiting inductors, which are placed in series with shunt capacitor banks in each phase, is discussed in detail. The primary purpose of these inductors is to limit the transient currents caused by the energization of the capacitor bank and the discharge current of the capacitor bank in the event of nearby faults. In banks with star connection, said inductors are placed between bus and circuit breaker, circuit breaker and capacitor or neutral point and capacitor in each phase. Since the primary purpose of these fixed inductors is to limit the transient currents associated with the capacitor bank, they are called transient limiting inductors.

In general, these inductors are introduced as damping inductors in the IET literature, current-reducing inductors in common use in the US, and for inductors used to limit large fault currents, and transient limiting inductors, which is the choice of the IEEE capacitor subcommittee.

In [3], firstly, national and international standards and authoritative articles related to the removal of destructive effects caused by transient currents caused by shunt capacitor banks and considerations for the use of transient limiting inductors in shunt capacitor banks were reviewed and then based on the IEC standard [5], reference article [1] and IEEE standard [4, 6-11].



(a)

(b)

Fig. 1: (a) The inrush current caused by the transient state of the capacitor bank connected back-to-back, (b) The transient current caused by the discharge of the energy of the capacitor bank in the condition of the occurrence of an external fault

In the paper [12], first, the capacitor current is accurately calculated when the capacitor bank is placed in the circuit, and the constant component and the transient component of the capacitor current are obtained, respectively. Then, a pre-charge strategy is proposed to reduce the inrush current caused by the capacitor being placed in the circuit according to the calculation results. The proposed strategy can make the transient component of the current at the closing moment zero or minimal. Then a pre-charge strategy for single-phase, two-phase and three-phase pre-charge is proposed and the topology of the pre-charge device is presented based on the target value. Finally, a PSCAD simulation model is built to validate the proposed precharge strategy. The simulation results show that the inrush current can be limited below 1.7 p.u. Also, the duration of the temporary closure has been greatly shortened. Thus, the effectiveness of the proposed pre-charge strategy is confirmed.

In the article [13], simulation has been done to study the inrush current characteristics of capacitor bank switching in Indonesia. The simulation results show that the inrush current for switching meets the IEC standard. However, for back-to-back switching, the inrush current exceeds the standard limit. With measurement data, the value of contact resistance for CB with back-to-back switching condition for each phase has a very different value and tends to fail. To reduce the inrush current, the use of damping inductor has been studied and the results show that the damping inductor can minimize the amount of inrush current by setting the correct value of the inductance of the damping inductor related to the reactive power of the capacitor bank.

In reference [14], in order to reduce the inrush current of shunt capacitors, the mathematical model of the real system in the shunt capacitor placement circuit has been created. The strategy in the three-phase shunt capacitor placement circuit is calculated when the inrush current is minimum and the effectiveness of the strategy is verified. The mechanical closing of the breaker is analysed. The measurement error of the synchronous voltage, the error reduction method is presented, and the closing delay is calculated to ensure that the shunt capacitor can be closed accurately at a certain time, and the impact of the closing current of the shunt capacitor on the power system is reduced.

1.3. Motivation

In this article, according to the standard IEC 62271-100 and, of course taking into account the supplementary materials from standards [4,5,7], a comprehensive algorithm for calculating the transient currents caused by the single capacitor bank switching, back-to-back capacitor bank switching and the discharge of the capacitor bank [1,8] is extracted.

The advantage of this algorithm is calculating the mentioned currents without computer simulation. Of course, it is worth mentioning that the outputs of this algorithm have been discussed and investigated by conducting computer simulations of sample substations in the EMTP-RV environment, which will be discussed in this article. Finally, the mentioned algorithm is completed by adding the

necessary criteria for the transient limiting inductor based on the IEC standard, in such a way that by receiving information from the power network, it is possible to reach the output of the utility value of the inductor after the implementation of the proposed algorithm. Also, if the inductor is not installed, it is possible to obtain the required amount of inductor based on the proposed algorithm.

1.4. Contribution

The algorithm presented in this article is based on [15] which reviews the single-line diagram of Khuzestan province substations and concludes that we are able to develop a software called Transient Analyzer to determine the amount of the series reactor of shunt capacitor banks in the power grid. The information of 20 substations studied in Khuzestan province was simulated by EMTP-RV software and its results were used to verify the designed algorithm. The software is highly efficient compared to the conventional simulation method and can be used with simple data entry and fast processing and presentation of results and data analysis in a short time.

2. REQUIREMENTS FOR SHUNT CAPACITOR BANK SWITCHING BASED ON STANDARD IEC STD 62271-100

The IEC committee develops standards and guidelines which are constantly updated. For this reason, it is essential to have access to the latest relevant instructions. Additionally, due to the continuous technical advances in the field of circuit breakers, it is essential to obtain the recommendations of the equipment manufacturer regarding the transient current capabilities of the circuit breaker. In general, two circuit breaker parameters are mentioned in the IEC standard [4] for shunt capacitor bank circuit breakers, 1) peak value of transient current and 2) frequency of transient current. In this standard, the exact requirements have been considered for all circuit breakers at all voltage levels; 1) The inrush current peak is less than or equal to 20 kA (i_peak≤20 kA) and the inrush current frequency is less than or equal to 4.25 kHz (f≤4.25 kHz). It is worth noting that in IEEE standards [9-11], the requirements of capacitor bank switching are given, which are different for every voltage level than the IEC standard, which is the same for different voltage levels.

3. CIRCUIT DIAGRAM FOR CAPACITOR BANK SWITCHING CALCULATIONS BASED ON STANDARD IEEE STD C37.012

The circuit diagram that is conventionally considered to perform capacitor bank switching calculations, as an example for the capacitor bus with the presence of two capacitor banks, is shown in Fig. 2. The transient current limiting inductance consists of the bus inductance between the switches, L_{bus}, the inductances between the switches and the capacitor banks, L_1 and L_2, the inductances of the capacitor banks, L_{c1} and L_{c2}, and any additional inductance. The total sum of the inductance between the capacitor banks, $L_{c1} + L_1 + L_{bus} + L_2 + L_{c2}$, is very small compared to the source inductance, L_s. In most cases, the total inductance is less than 1% of the source inductance, and the contribution of the source inductance to the back-to-back switching inrush current is negligible [5]. However, regarding the switching of a separate capacitor bank, the said inductance has a dominant effect. In connection with the external network, to perform switching calculations, the said network is replaced with the Tonen equivalent circuit including voltage source and short circuit impedance (L_s) as source inductance. The capacitor bank itself is not simple. But, in general, its value is in the order of 10 μH and 5 μH for banks with a voltage higher than 52 kV and lower than 52 kV, respectively. In Table 1, for different voltage levels, the conventional values of inductance between capacitor banks are given [4].

Transients are the result of sudden changes in the power grid. Opening or closing a circuit breaker changes the topology of the network and the related flows. It always takes a period for the network conditions to stabilize after the changes as mentioned earlier. All transients occur due to electrical connection or disconnection in the power grid or energy injection through lightning strikes or static discharges. In the following, it will be introduced how to calculate the size and frequency of the inrush currents caused by electrifying the capacitor bank and discharging the current of the capacitor bank.

3.1 Inrush currents caused by energizing shunt capacitor banks

Energizing the capacitor bank by the circuit breaker creates a connected inrush current, which is a function of the applied voltage, the value of the capacitor's capacity, the value of the inductance of the connected path, and the remaining charge of the capacitor at the moment of the circuit connection. In general, there are two different scenarios for energizing capacitor banks in shunt.

- Energizing a single capacitor bank
- Back-to-back energization of the capacitor bank

The connected inrush current in a charged capacitor bank can be higher than in an uncharged (uncharged) capacitor bank, depending on the polarity of the main voltage and the remaining charge on the capacitor. Calculating the value of peak inrush current and the corresponding frequency can be done relatively simply by assuming that the capacitor bank is discharged and connected when the maximum inrush current is produced.

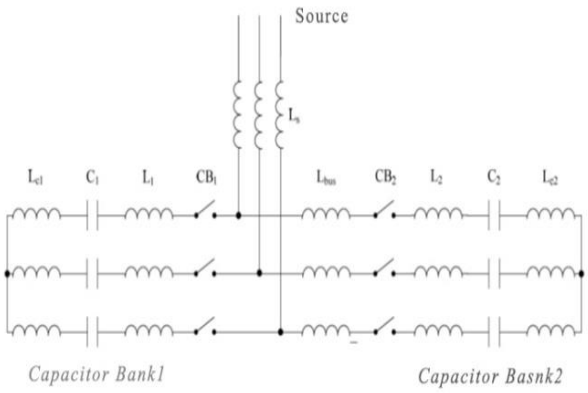


Fig. 2: Conventional circuit for switching calculations of two capacitor banks [4].

It is always assumed that the capacitor bank has been discharged before it is energized. This assumption is reasonable. The reason for this is the existence of discharge resistors in the capacitor bank building. Conventionally, the duration of the discharge of the capacitor bank is within 5 minutes [4].

4. The inrush current of a single capacitor bank switching transient

The switching phenomenon of a single capacitor bank can be well understood through Fig. 2. As it can be seen from the circuit theory, after connecting the switch in the circuit of Fig. 3, the current flows in the circuit, and this current has two components: constant and transient. The mentioned transient current will have the highest amplitude when the switch closing action occurs at the peak of the voltage wave. If the voltage wave is sinusoidal, the transient current component will be in (1) [6].

$$\mathrm{i}(t) = i_{i\,peak} \times e^{-\frac{R_s}{L_s}t} \times \sin \omega_i t \tag{1}$$

where R_s is the source series resistance, L_s is the inductance of the source series, and $i_{i\,peak}$ is the peak value of the passing current. Also, $f_i = 1/2\pi\sqrt{(L_s C_1)}$ is the frequency of the inrush current of the circuit, and because the ohmic resistance of the circuit is relatively small, the value of the transient current peak is determined by the wave impedance of the circuit, Z [6].

$$i_{i\,peak} = \frac{\sqrt{2}u}{Z} = \sqrt{2}u \times \sqrt{\frac{C_1}{L_s}} = U \times \sqrt{\frac{2}{3}\frac{C_1}{L_s}} \tag{2}$$

Where u is the single-phase RMS voltage, U is the nominal line-to-line voltage of the network, and C_1 is the capacitor bank value. Also, the value of the peak capacitance current of the constant component is obtained from (3) [6].

$$\sqrt{2} \times i_1 = \sqrt{2}u \times \omega C_1 = \sqrt{\frac{2}{3}} \times U \times \omega C_1 \tag{3}$$

where ω and i_1 are the effective value of the permanent capacitor current and the value of the grid frequency, respectively.

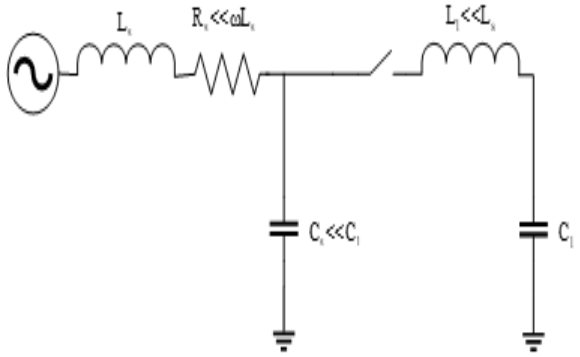


Fig. 3: Simplified circuit diagrams of the single capacitor bank: Cs (dissipation capacitor), Rs (source-series resistance), and Ls (source-series inductance) circuit parameters on the grid side, C1 and L1 are circuit parameters on the capacitor bank side [5].

From the ratio of peak currents of constant and transient components from (2) and (3), the following relation will be obtained [6]:

$$\frac{i_{i\,peak}}{\sqrt{2} \times i_1} = \frac{1}{\omega\sqrt{L_s C_1}} = \frac{\omega_i}{\omega} = \frac{f_i}{f} \tag{4}$$

Also, if I_{sc} is considered as the RMS value of the nominal short circuit current, equation (2) and the frequency of the inrush current can be written as (5) and (6) [6]:

$$i_{i\,peak} = \sqrt{2}\sqrt{I_{sc} i_1} \tag{5}$$

$$\omega_i = \omega \sqrt{\frac{I_{sc}}{i_1}} \tag{6}$$

Specifically based on Fig. 3, the power of a single-phase short circuit in the capacitor bank busbar is equal to [6]:

$$P_k = \frac{u^2}{\omega L_s} \tag{7}$$

Moreover, the power of single-phase capacitor bank is equal to [4]:

$$P_C = u^2 \omega C_1 \tag{8}$$

The ratio of the equations (7) and (8) is equal to [6]:

$$\frac{P_k}{P_C} = \frac{1}{\omega^2 L_s C_1} = \frac{\omega_i^2}{\omega^2} = \frac{f_i^2}{f^2} \tag{9}$$

which can be written using (4) and (9):

$$\frac{i_{i\,peak}}{\sqrt{2} \times i_1} = \sqrt{\frac{P_k}{P_C}} \tag{10}$$

Equations (9) and (10) show that the peak value of the transient component of the current is usually higher than the peak value of the steady component of the current. In the IEEE standard [4], it is pointed out that the peak value of the transient current component is usually about 20 times the peak value of the constant current component.

5. Back-to-back Capacitor Bank Switching Inrush Current

The energization of one capacitor bank while the other adjacent capacitor bank is in service is known as back-to-back switching. By increasing the number of shunt capacitor banks in service, the amplitude and frequency of inrush current flowing between the capacitor banks increases. To understand the back-to-back switching phenomenon, we can consider Fig. 4. In this figure, the capacitor bank C_2 is in the circuit before the capacitor bank C_1 is energized. By putting the equivalent capacitor and the equivalent series inductance in equation (2) and the equation $f_i = 1/2\pi\sqrt{(L_s C_1)}$, the equations (11) and (12) will be obtained [4]:

$$i_{i\,peak} = \sqrt{2} \times u \times \sqrt{\frac{C_{eq}}{L_{eq}}} = U \times \sqrt{\frac{2}{3} \times \frac{C_{eq}}{L_{eq}}} \quad (11)$$

$$f_i = \frac{1}{2\pi\sqrt{C_{eq} \times L_{eq}}} \quad (12)$$

$$C_{eq} = \frac{C_1 \times C_2}{C_1 + C_2} \quad (13)$$

$$L_{eq} = L_1 + L_2 \quad (14)$$

Considering the two equations $i_1 = u \times \omega C_1$ and $i_2 = u \times \omega C_2$ as permanent currents of two capacitor banks, equations (15) and (16) can also be considered for the peak inrush current and its frequency [4].

$$i_{i\,peak} = \sqrt{2} \times u \times \sqrt{\frac{i_1 i_2}{u\omega L_{eq}(i_1 + i_2)}} = \sqrt{2} \times \sqrt{\frac{u i_1 i_2}{\omega L_{eq}(i_1 + i_2)}} \quad (15)$$

$$f_i = \frac{1}{2\pi} \times \sqrt{\frac{\omega u(i_1 + i_2)}{L_{eq} i_1 i_2}} = \frac{1}{2\pi} \times \sqrt{\frac{2\pi f u(i_1 + i_2)}{L_{eq} i_1 i_2}} \quad (16)$$

Also, considering $C_2 = aC_1$ in which $a \geq 1$ means $C_2 \geq C_1$ and $L_2 = \frac{L_1}{a}$ from equations (11) and (12), equations (17) and (18) will be extracted [5]:

$$i_{i\,peak} = \sqrt{2} \times u \times \frac{a}{a+1} \times \sqrt{\frac{C_1}{L_1}} = \sqrt{\frac{2}{3}} \times U \times \frac{a}{a+1} \times \sqrt{\frac{C_1}{L_1}} \quad (17)$$

$$f_i = \frac{1}{2\pi\sqrt{L_1 C_1}} \quad (18)$$

Comparing (4) and (17), it can be seen that the inrush current of capacitor bank C_1, i.e., (17), can be expressed as a function of the constant component of the first bank current [5].

$$i_{i\,peak} = \frac{a}{a+1} \times \frac{f_i}{f} \times \sqrt{2} i_1 \quad (19)$$

Equation (19) is used in practice to calculate the transient component of the inrush current of back-to-back capacitor banks with two or more banks.

Capacitance banks with n+1 branches, according to Fig. 5, can first be combined as equivalent to two capacitor banks and then using equations (11) and (12), provided that L_2 and C_2 from Fig. 3 with the following parameters should be replaced [5].

$$L' = \frac{1}{\sum_{j=(n+1)}^{j=1} \frac{1}{L_j}} = \quad (20)$$

$$C' = \sum_{j=(n+1)}^{j=2} C_j \quad (21)$$

6. Outrush Current of Capacitor Banks

In the condition that there is a fault near the shunt capacitor bank(s) at the substation and one of circuit breakers at the beginning of the adjacent feeder is closed in the presence of the fault (for example, during the single-pole reclosing, in addition to the main current component, another current component with the frequency and a significant amount will pass through the mentioned switch, which is the outrush current of the capacitor bank in the fault location. Fig. 6 shows an example single-line diagram that calculate the value and frequency of outrush current in the presence of a single capacitor bank [1]. The peak value of the capacitor bank outrush current, and its frequency can be calculated based on the diagram shown in Fig. 6 through the following equations [1, 7, 8]:

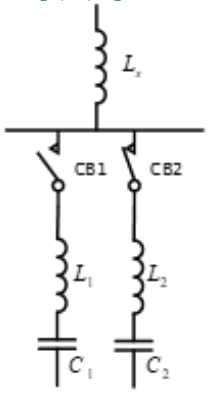


Fig. 4: Circuit diagram of two back-to-back capacitor banks [5].

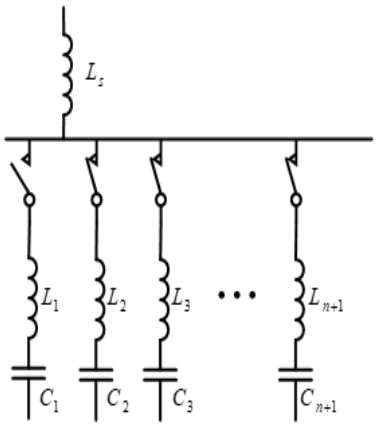


Fig. 5: Back-to-back n+1 capacitor banks diagram [5].

$$L_{eq} = \frac{1}{\sum_{j=(n+1)}^{j=1} \frac{1}{L_j}} \quad (22)$$

$$C_{eq} = \sum_{j=(n+1)}^{j=1} C_j \quad (23)$$

$$f_i = \frac{1}{2\pi\sqrt{(L_{adj} + L_{eq})(C_{eq})}} \quad (24)$$

$$i_{\mathrm{pk_i}} = V_o \times \sqrt{\frac{2}{3} \times (C_{eq}) \times \frac{1}{(L_{adj} + L_{eq})}} \quad (25)$$

In these relationships, i_{pk} is the maximum outrush current (kA), f_i is the transient current frequency of discharge of the capacitor bank, V_o is equal to the line voltage, L_{adj} is the inductor at the beginning of the adjacent feeder in the bus location, and the fault location, L_{eq} is the equivalent inductor of the branches of the capacitor bank (including the bank inductor) The capacitor is our capacitor between the capacitor bank and the beginning of the bus, and C_{eq} is the equivalent capacitance of the capacitor banks. For shunt capacitor banks, a reasonable estimate of the outrush current can be calculated as follows [7]:

$$i_{pk} = \sqrt{\frac{1000}{3f}} \times \sqrt{\frac{Q_C\ kvar}{L}} \quad (26)$$

where i_{pk} is the maximum outrush current (kA), f is the frequency of the power system, Q_C is the three-phase nominal reactive power of the capacitor bank, and L is the inductance between the capacitor bank and the fault location (μH).

7. An Algorithm for Determining the Usefulness of Transient Limiting Inductors

Fig. 7 shows the flowchart of the comprehensive algorithm for determining the desirability of the limiting inductor [12]. The steps of implementing the algorithm are as follows:

Step 1: In this step, the inrush current $i_{sb}(i)$ and its oscillation frequency $f_{sb}(i)$ in the scenario of connecting a single capacitor bank for each capacitor bank are calculated using (2) and (4).

Step 2: In this step, the suitability of the calculated values is checked according to the IEC62271-100 standard. In other words, it is checked that the range of inrush current is less than 20 kiloamperes, and the frequency of its fluctuations is less than 4250 Hz.

Step 3: In this step, the inrush current $i_{b2b}(i)$ and its fluctuation frequency $f_{b2b}(i)$ in back-to-back scenarios are calculated based on (11), (12), (20), and (21).

Step 4: In this step, similar to the second step, according to the IEC standard, the suitability of the values calculated in the third step is checked.

Step 5: In this step, the inrush current $i_{outrush}(i)$ and its oscillation frequency $f_{outrush}(i)$ in the capacitor bank discharge scenario in the condition of near-fault occurrence are calculated using (22) to (25).

Step 6: In this step, similar to the second, and fourth steps, according to the IEC standard, the suitability of the values calculated in the fifth step is checked.

It is worth mentioning that in each of the second, fourth and sixth steps, according to the standard [3], the inrush current, and calculated frequency are compared with the allowed values. If the calculated current and frequency are not in the allowed range, by increasing the TLI inductance value specified under Ladd, calculations are calculated again with the new inductance and this repetition loop continues until the current and frequency are within the allowed range. Finally, Ladd is considered to be the minimum inductance required for the inductor to be optimal.

8. Simulation and Discussion

In this section, the studied network modeling report in EMTP-RV software and the evaluation of the proposed comprehensive algorithm are given.

8.1. Networks Modelling

Fig. 8 shows the single-line diagram of a studied substation including two shunt capacitor banks with a nominal power of 4.8 MW. In this substation, two capacitor banks are connected to the 33 kV bus. Also, the nominal specifications of each circuit breaker are:

- The nominal voltage of the switches is 36 kV.
- The nominal short-circuit current of the circuit breakers is equal to 25 kA.
- $\boldsymbol{L_1}$ and $\boldsymbol{L_2}$ are the inductance between the bus and the capacitor bank circuit breaker
- $\boldsymbol{L_3}$ and $\boldsymbol{L_4}$ are the inductance between the capacitor bank circuit breaker and the capacitor bank
- $\boldsymbol{L_{BUS1}}$ *and* $\boldsymbol{L_{BUS2}}$ are the inductance of the bus path between circuit breakers.

First, this network was modeled in EMTP-RV software. Then, different capacitor bank switching scenarios were simulated through the 5512 CB.

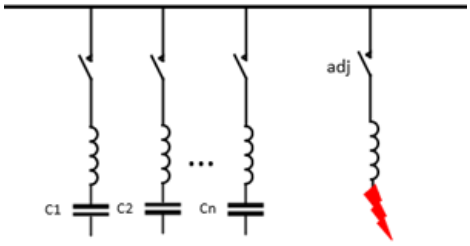


Fig. 6: System diagram to evaluate the capacitor bank outrush current [2].

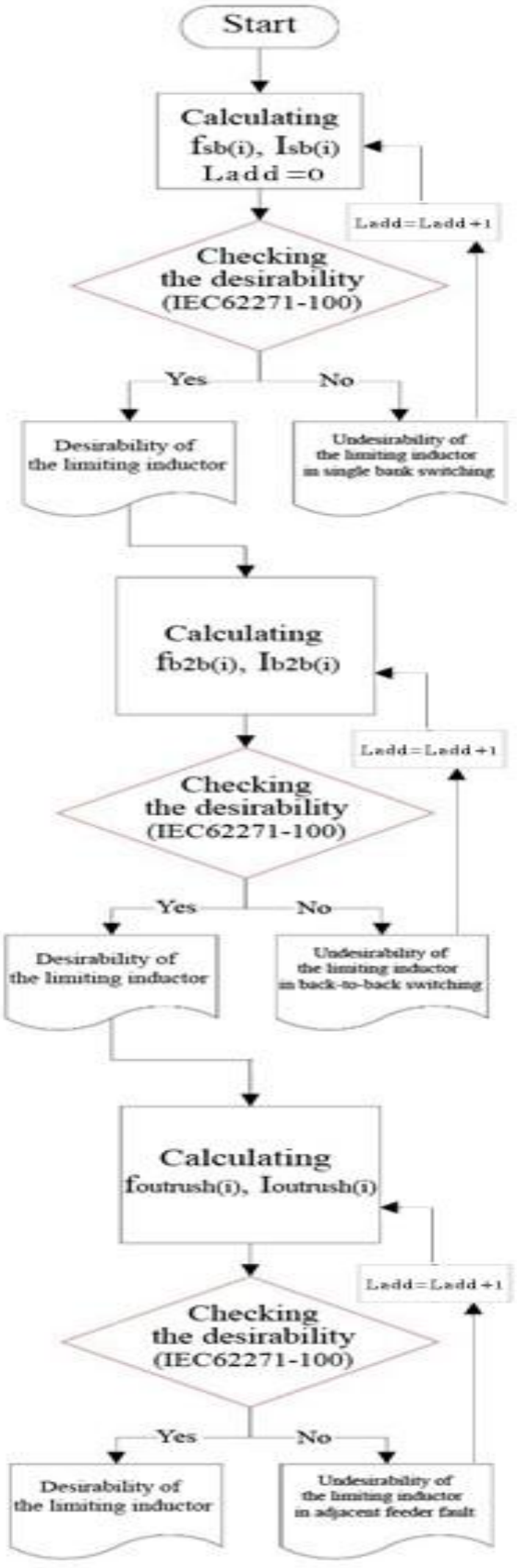


Fig. 7: Comprehensive algorithm for determining the desirability of transient limiting inductor.

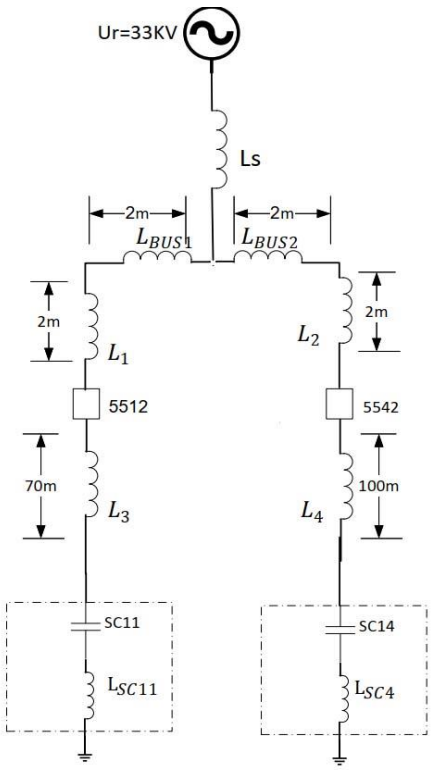


Fig. 8: Single-line diagram of 33 KV studied substation.

8.2. Comparison of EMTP-RV Results and Proposed Algorithm

In Tables 2 and 3, respectively, the results obtained from checking the suitability of the transient limiting inductor concerning the transient states of capacitor bank switching in the studied substation with the EMTP-RV software and the proposed algorithm can be seen. As can be seen, the peak current and frequency values using the proposed algorithm in Table 2 are very close to the corresponding values in Table 1.

The current waveform obtained from the transient states in the EMTP-RV software is shown in Figs. 9, 10 and 11.

Table 1: Conventional inductance values between capacitor banks [4].

Maximum rated voltage (kV)	Bus bar inductance per phase ($\frac{\mu H}{m}$)	Conventional inductance between banks* (μH)
17.5 and below	0.702	10 to 20
36	0.781	15 to 30
52	0.840	20 to 40
72.5	0.840	25 to 50
123	0.856	35 to 70
145	0.856	40 to 80
170	0.879	60 to 120
245	0.935	85 to 170

* This value does not include the inductance of the capacitor bank itself. In total, the inductance of the capacitor bank is in the order of 10 µH and 5 µH for banks with a voltage higher than 52 kV and lower than 52 kV.

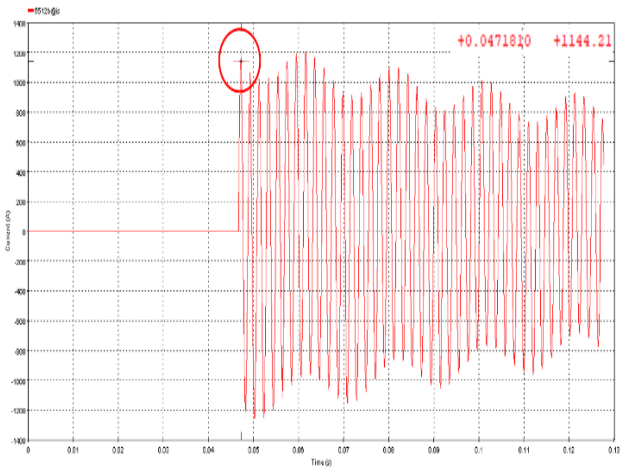


Fig. 9: The single bank switching current waveform of SC11.

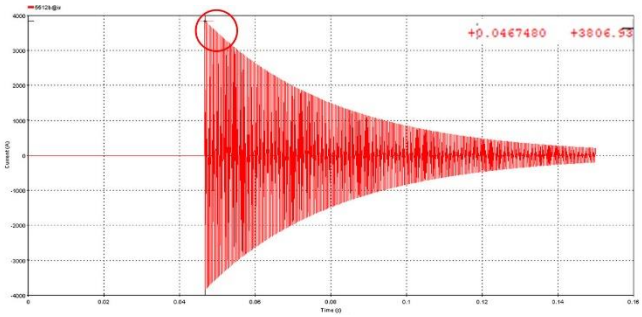


Fig. 10: The back-to-back switching current waveform of SC11 (EMTP-RV).

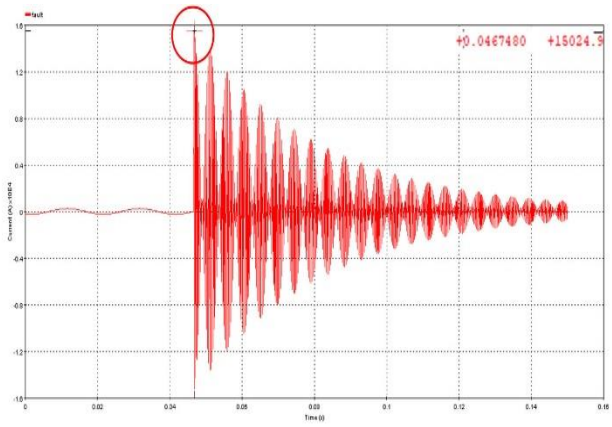


Fig. 11: Outrush current waveform (EMTP-RV).

Table 2: Evaluation Results for the network by EMTP-RV.

Scenario	Peak current (kA)	Current frequency (Hz)	Amount of inductor
Single-bank switching SC11	1.144	484	Desirable
Back-to-back switching SC11	3.806	3209	Desirable
Outrush current	15.024	3215	Desirable

Table 3: Evaluation results for the network by the proposed algorithm.

Scenario	Peak current (kA)	Current frequency (Hz)	Amount of inductor
Single bank switching SC11	1.150	486	Desirable
Back-to-back switching SC11	3.840	3231	Desirable
Outrush current	15.280	3224	Desirable

The comparison of the results of Tables 1 and 2 can be seen in Fig. 12 in a more specific way. Another point that can be mentioned in Tables 1 and 2 is the result of examining the usefulness of the transient limiting inductor, obtained with both methods of the same output in this connection.

9. Development of Software

9.1. Methodology

The production and development of a software package requires step-by-step actions that can finally be presented in the form of efficient, and standard software. Therefore, in the following, the method used in producing the software package is explained in 5 steps. These steps can be seen in Fig. 13.

9.2. Design and Implementation of Database Based on Database Management System

Using the database management system provides the possibility of editing, deleting, and adding data in the future. if the volume of input data is high, they can be saved for later use. Therefore, since substations may undergo changes in development plans and need to be updated or add new data, it is necessary to design the data in a database that can be managed or edited. Therefore, MySQL data management system has been used in the design and implementation of this software package.

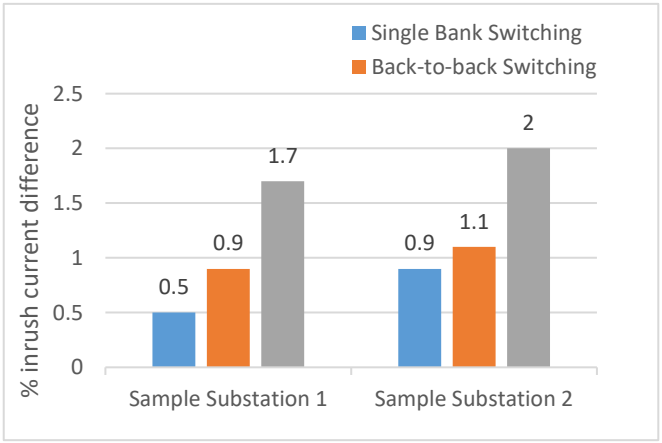


Fig. 12: The percentage difference between the transient current value in EMTP-RV software and the proposed algorithm.

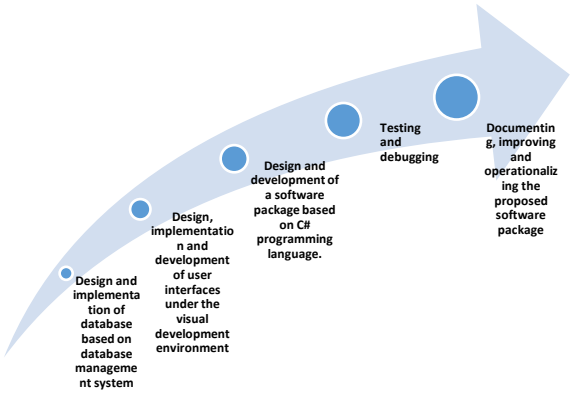


Fig. 13: Action diagram for software development to determine the desirability of transient limiting inductors for shunt capacitor banks.

Before designing the database, the processes and algorithms were checked, and then the database tables were designed according to the data and the relationship between them. The relationship between the tables was determined differently to avoid redundancy and repetition of data. One of the most fundamental challenges in developing a database is determining the exact relationship between data tables. Accurate knowledge of the nature of the data, as well as complete knowledge of the processing algorithms in which the data are used, are among the factors that influence the determination of the relationship between the data tables. Therefore, the database model has been extracted by conducting numerous investigations regarding the exact knowledge of the nature of the data and how to use the processing algorithms. Next, as an example in Fig. 14, the structure of the data table of breakers is given.

In the first field, a numeric ID is assigned to each breaker, which is unique and cannot be empty, and in the second field, a name is assigned to each breaker, which is a string type and cannot be empty. In the third field (bb_id), this breaker is assigned to a busbar whose value is numerical and cannot be empty. In the field (i_sc_b), the value of the short circuit current is of decimal type and cannot be empty.

Tables are linked through foreign keys. Like the table of circuit breakers, which is linked to the table of busbars through the bb_id field and specifies the busbar to which the circuit breaker is connected. Also, when inserting data, it is necessary to validate the type of user input data so that they do not encounter errors when inserting into the database. Like the breaker short circuit current field that cannot be empty and must enter a numerical value, otherwise it will not be allowed to enter information in the database.

9.3. Design, Implementation, and Development of User Interfaces Under the Visual Development Environment

After compiling the database to communicate between the written algorithms, the database, and the user requests, a user interface is needed, and the visual development environment has been used to create this connection. In fact, by the user interface, the required data is received from the user and stored in the database, and then, according to the user's request for processing, the required data is called from the database tables, and its report is displayed through the user interface.

In Fig. 15, there is an example of a user interface that can add, delete, and edit data by clicking on its different parts. In Fig. 15, the user can add a new substation in the software through the designed user interface. Moreover, in Fig. 16, the user can perform the desired processing on the data stored in the database by selecting the processing method, the desired station, and voltage level.

9.4. Design and Development of a Software Package based on C# Programming Language

C# programming language has been used to develop the user interface and compile algorithms as well as to communicate with the database in the visual environment. This language has several advantages, including:

1- Syntax similar to Java, C++, and C language

2- The most powerful programming language from Net Framework. Uses.

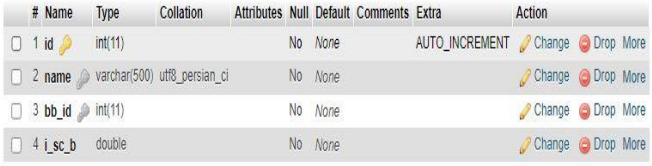
3- High security

4- Ability to reuse codes with rich libraries for use in different fields

5- Being multi-platform (Cross-Platform)

9.5. Testing and Debugging

After the initial compilation of the algorithms, receiving data from the database, and reporting the processes resulting from the implementation of the algorithms, it is necessary to create test data to test and check the performance of the software in different conditions and display possible errors to the user; In order to ensure the correct implementation of the obtained algorithms, when using the software, the user can perform the desired processing and receive a favorable report by receiving the appropriate message and correcting the data.



#	Name	Type	Collation	Attributes	Null	Default	Comments	Extra	Action
1	id	int(11)			No	None		AUTO_INCREMENT	Change Drop More
2	name	varchar(500)	utf8_persian_ci		No	None			Change Drop More
3	bb_id	int(11)			No	None			Change Drop More
4	i_sc_b	double			No	None			Change Drop More

Fig. 14: Table structure of data breakers in MySQL database

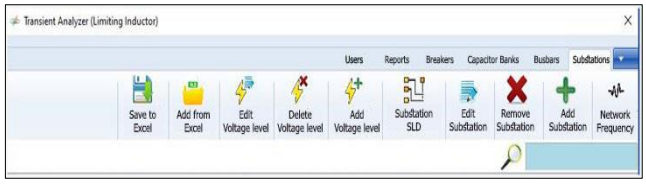


Fig. 15: Sample user interface (main page of the software).



Fig. 16: User interface example (add substation).

Testing and debugging is one of the most extended steps in software production, because the suitability of all algorithms and models used in the software is examined according to the sample data, and the system messages to the user are determined and modified with great accuracy and sensitivity; To avoid unforeseen ambiguities while using the software. This stage of developing the software package is repeated many times to fix all the tests and bugs of the software. Figs. 17 and 18 show examples of error messages in adding a station and a breaker, respectively. Fig. 19 shows the steps taken in the testing and debugging stage of the software. After preparing the initial version of the software package, the sample data has been entered into the software. Software bugs, including error notification when entering incorrect information as well as during data processing, matching the output of the coded algorithm in the software with the manually calculated results, and then the solution is determined by holding joint meetings between the computer group and the electrician. Applications are provided to report errors and modify algorithms. Moreover finally, the solutions provided in the software have been applied, and a new version has been provided. These measures have been continued until all the problems have been resolved and corrective measures have been implemented during numerous meetings.

9.6. Documenting, Improving, and Finalizing the Proposed Software Package

In order to finalize the software, user interfaces, and graphical interfaces for data entry, the selection of processing operations and reporting were reviewed. The arrangement of graphic elements, and data entry steps was modified so that the user could quickly enter the data and get the desired output from the software. The software report was modified according to the user's needs. Primary data and graphic charts were applied in the report to understand the results of the processes better. In order to improve the application of the software in organizations and its use by several users, the user management section has been added to the software, which allows the definition of new users with different accesses. This way, each user can enter data from different stations, perform processing operations, and get reports from the software.

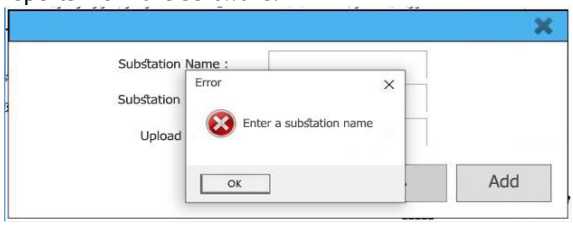


Fig. 17: Sample error message when adding a substation.

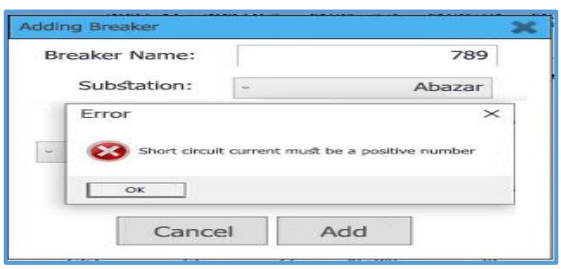


Fig. 18: Sample message when adding a breaker.

The user management section is shown in Fig. 20. It is possible to add, delete, and edit users. In the section of the main page of user management, it is possible to search among users and the time of their last login. To document and improve the use of the software, a user guide was developed. In this guide, how to work with all the menus, as well as how to enter data, perform processing operations, and report from the software, are illustrated. Figs. 21 and 22 are examples of software manual pages.

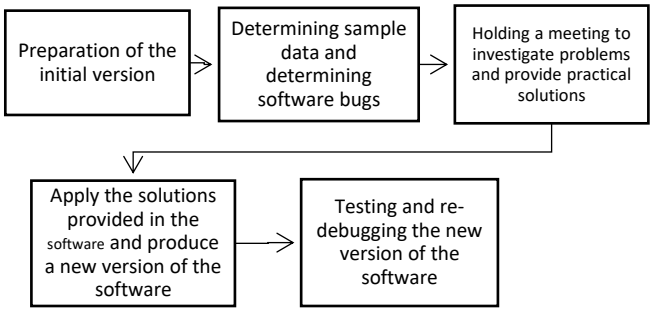


Fig. 19: Diagram of software testing and debugging procedures.

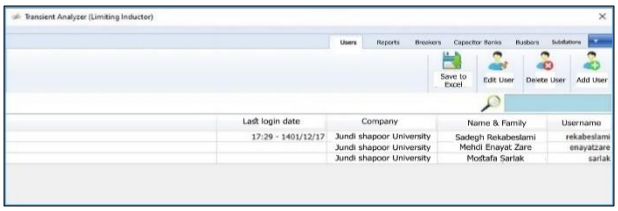


Fig. 20: User management section in Transient Analyzer software.

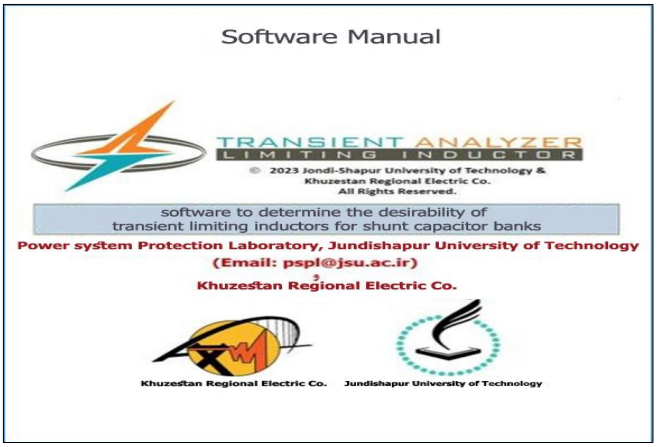


Fig. 21: Transient Analyzer software manual.

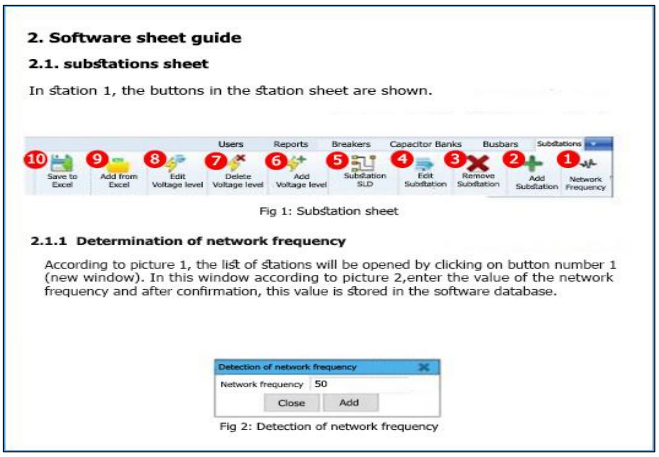


Fig. 22: Transient Analyzer software manual.

10. PRACTICAL EXAMPLE

In the following, Shadegan substation network is considered as a sample network to check the desirability of series inductors with the help of the proposed software.

10.1. Case Study

Fig. 23 shows the diagram of Shadgan substation, including a bank of shunt capacitor banks with a rated power of 4.8 MW. In this station, two capacitor banks are connected to the 33 kV bus. Also, the nominal specifications of each of the circuit breakers are:

- The nominal voltage of circuit breakers is 36 kV.
- The nominal short-circuit current of circuit breakers is equal to 25 kiloamperes.
- **L_1** and **L_2** are the inductance between the bus and the circuit breaker of the capacitor bank.
- **L_3** and **L_4** are inductance between the capacitor bank circuit breaker and the capacitor bank.
- **L_{BUS1}** and **L_{BUS2}** are the inductance of the bus path between circuit breakers.

Network information:

U_r	33 kV
L_s	The inductance of the source is equal to 7.5 mH and according to the frequency of 50 Hz, it is equivalent to 2.385 ohms.
L_1, L_2	The inductances between the bus and the circuit breaker of each capacitor bank
L_3, L_4	Inductances between capacitor bank circuit breaker and each capacitor bank
L_{BUS1} و L'_{BUS2}	Bus inductance between capacitor bank circuit breakers.
L_{sc11}, L_{sc12}	Inductance of each phase in each capacitor bank.
5512,5522	circuit breakers
	The short circuit current of the source (I_s) is equal to 8.774 kA at a voltage of 33 kV.

10.2. Investigating the Desirability of Transient Limiting Inductors of Sample Networks Using the Proposed Software

The information under Sections 1-3 is entered in the Transient Analyzer software and after all the processes are done, the software report is presented in Figs. 24 and 25. Fig. 24 shows the characteristics of the desired station, and Fig. 25 shows the results of the processing done by the developed software.

As shown in Fig. 25, the results of single capacitor bank reconnection processes are favorable according to the IEC Std62271-100 standard. However, the results of back-to-back capacitor bank connection processes are unfavorable according to the standard, and up to 78 microHenries are required for the limiting inductor. The series should be added so that the results are favorable. Also, the results of capacitor bank energy discharge processes in the conditions of near external fault occurrence are unfavorable according to the standard criteria, and it is necessary to add 78 µH to the series limiting inductor to make the results favorable. Therefore, in total, if 78 µH of inductance is added to the series inductor, the results will be favorable in all three scenarios.

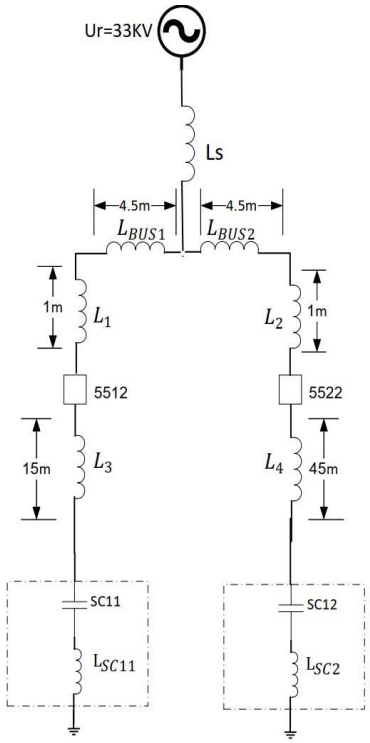


Fig. 23: Single-line diagram of 33 KV substation.

Processing results of the desirability of transient limiting inductors in shunt capacitor banks

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1. General specifications

User specifications	Name & Family	Company	Date & Time
Manager System	Sadegh Rekabeslami	Jundi Shapoor University	1401/09/12 9:21

2. Specifications of substation

Substation	Short circuit current (A)	Short circuit Reactance (ohm)	Frequency (Hz)	Substation Position	Short circuit power (MVA)
Shadegan	-	2.383	50		-

3. Specifications of selected busbars

Busbar	Voltage level (Kv)	Adjacent breaker	Distance of adjacent feeder from busbar(m)	Short circuit current of adjacent feeder (kA)
51	33	5022	1	25
52	33	5042	1	25

4. Specifications of capacitor banks

Capacitor bank	Voltage Level (Kv)	Reactive power (MVA)	Limiting inductance (uH)
SC11	33	4.8	0
SC12	33	4.8	0

5. Specifications of circuit breakers

Breaker	Breaker Short circuit current (kA)	Distance of breaker to source (m)	up stream case	Distance to upstream case (m)	downstream case	Distance to downstream case (m)
5512	25	5.5	51 Busbar	5.5	SC11	20
5522	25	5.5	52 Basbar	5.5	SC12	14

Fig. 24: Software report - Shadgan station specifications.

6.1. Investigating the desirability of series limiting inductors at the voltage level of 33 kV

6.1.1. The results of single capacitor bank switching processes

Min Additional TLI * (uH)	Desirable limiting inductor (IEC Standard 62271-100)	Frequency (Hz)	Current Peak (KA)	Capacitor Bank	Breaker
-	Desirable	487.05	1.16	SC11	5512
-	Desirable	487.20	1.16	SC12	5522

6.1.2. The results of back-to-back capacitor bank switching processing

Min Additional TLI * (uH)	Desirable limiting inductor (IEC Standard 62271-100)	Frequency (Hz)	Current Peak (KA)	Capacitor Bank	Breaker
78	Undesirable	8.943	10.62	SC11	5512
78	Undesirable	8.943	10.62	SC12	5522

6.1.3 The results of capacitor bank energy discharge processes in near fault conditions

Min Additional TLI * (uH)	Desirable limiting inductor (IEC Standard 62271-100)	Frequency (Hz)	Current Peak (KA)	Busbar	Adjacent breaker
78	Undesirable	8.692	41.30	51	5022
78	Undesirable	8.692	41.30	52	5042

6.2. Analysis of 33 kV voltage level processes

Min Additional TLI * (uH)	Desirable limiting inductor (IEC Standard 62271-100)	Voltage level (Kv)	Substation
78	Undesirable	33	Shadegan

Fig. 25: The results of Shadgan station processing algorithms.

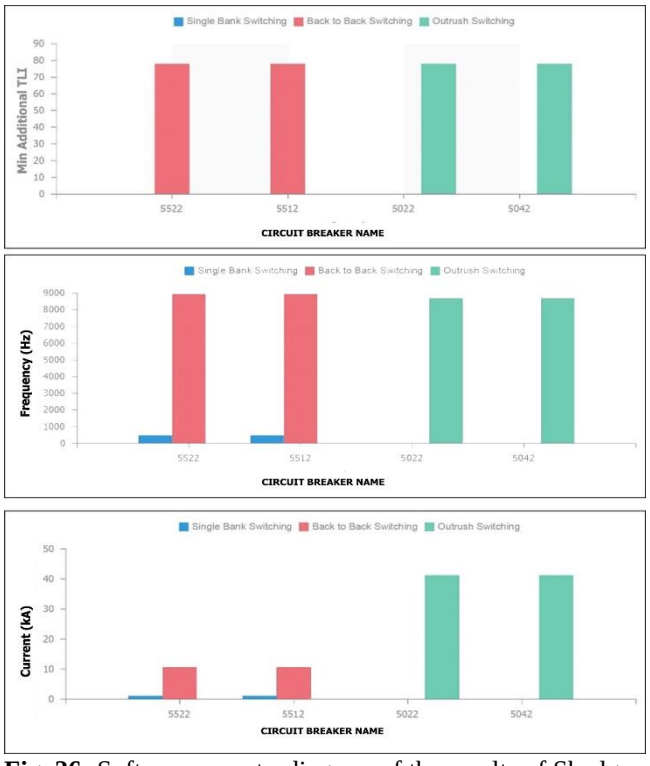


Fig. 26: Software report - diagram of the results of Shadgan station's processing algorithms.

Fig. 25 shows the report of software processing algorithms in Shadgan station. The inrush current and its frequency and minimum inductor have been compared for the suitability of conduit capacitor bank switching scenarios, back-to-back, and capacitor bank discharge in the near-fault location.

11. Conclusion

In this article, based on IEC standards for shunt capacitor banks, using nominal information of circuit breakers, capacitor banks, the distance between the installed equipment and the corresponding busbar short circuit level, a comprehensive algorithm for determining the desirability of the value of transient limiting inductors in capacitor banks was tried. Then, according to the comparison of the results of the developed algorithms with the results of the EMTP-RV software, the validation of the proposed algorithm was done, and it was observed that the difference percentage is less than 2%. Therefore, the developed proposed algorithm has good accuracy compared to EMTP-RV software. Also, the methodology of developing and producing software for determining the desirability of shunt capacitor bank series inductors was investigated. In the end, the proposed algorithm was released in a software package called ‹Transient Analyzer for ease of use.

Credit Authorship Contribution Statement

Sadegh Rekabeslami Zadeh: Conceptualization, Data curation, Formal analysis, Investigation, Methodology, Resources, Software, Validation, Roles/Writing - original draft. **Gholamali Torabi:** Data curation. **Sasan Najafi Birgani:** Conceptualization, Data curation, Formal analysis, Funding acquisition, Investigation, Methodology, Project administration, Resources, Software, Supervision, Validation, Visualization, Roles/Writing - original draft, Writing - review & editing. **Mehdi Enayat Zare:** Data curation, Formal analysis. **Mostafa Sarlak:** Conceptualization, Data curation, Formal analysis, Resources, Supervision, Writing - review & editing.

Declaration Of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper. The ethical issues; including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, redundancy has been completely observed by the authors.

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BIOGRAPHY



Sadegh Rekabeslami Zadeh received the B.S. degree in electrical engineering from Shahid Chamran University of Ahvaz (SCU), Khuzestan, Iran, in 2013 and the M.S. degrees in electrical engineering from Joundi-Shapour University of Technology (JSU), Dezful, Iran, in 2023, respectively. Currently, he is Electrical Expert in Khuzestsn Steel Company. His research interests include the application of the new methods of AI in power system studies.



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