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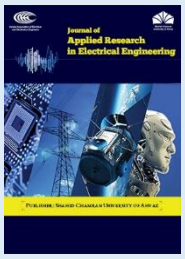

Research Article

Improving Power Quality Using a Fuzzy Inference System-Based Variable Forgetting Factor Recursive Least Error Square Control Scheme of DSTATCOM

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Abstract: A two-layer combined control method is developed for a four-leg Distribution Static Synchronous Compensator (DSTATCOM). The method aims at harmonics reduction, demand-generation equilibrium, power factor modification, voltage adjustment, and neutral current modification in a 3ph 4-wire distribution system. In the first layer, a recursive Least Error Square algorithm (RLES) based on a new fuzzy logic-based variable forgetting factor is used for Real-time estimation of voltage and current signals and their constituting components. The second layer's duty is to extract the reference currents using the outputs of the first layer. Besides the high accuracy and convergence speed, the suggested algorithm is independent of coordinate transformations and complex computation when attempting to derive the reference currents of DSTATCOM. To enhance the dynamic performance of DSATATCOM, an adaptive hysteresis band current controller was utilized to generate switching signals. The effectiveness of the presented control strategy was verified via simulation studies implemented in MATLAB/Simulink environment.

Keywords: DSTATCOM, Power Quality, Recursive Least Error Square, Fuzzy Logic Variable Forgetting Factor, Adaptive Hysteresis Band Current Control

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1. INTRODUCTION

Exponentially-increasing deployment of nonlinear loads has led to an elevation in the level of harmonic pollutions in the power grid, which creates many problems for performance, protection and control of electrical facilities. Nonlinear loads contain harmonic contents and draw reactive power from AC mains, causing power quality issues, especially voltage harmonics at the Point of Common Coupling (PCC), and thus, disrupting the load joined to the PCC [1, 2]. Harmonic estimation is one of the major aims of control systems. However, harmonic measurement is difficult because a majority of harmonic causes are inherently dynamic and contain voltage/current signals that vary over time. Thus, harmonic components should be estimated fast and accurately. This justifies the use of estimation algorithms which have less complexity for the real-time implementation [3].

Phase Lock Loops (PLL)-based control algorithms [4-6] are conventional methods for estimating harmonic components of disturbed power signals. However, under unbalanced or disturbed voltage conditions, PLL shows a phase delay, which leads to a slow response and equipment failure in the power system. Many researchers have investigated different solutions for PLL tracking capability and performance improvement, such as Delay-Based PLLs [7] and Frequency Fixed Second-Order Generalized Integrator- based PLL (FFSOGI-PLL) [8]. In general, a trade-off between fast tracking and proper filtering is applied in the PLL optimization methods. Most of these methods are very sensitive to harmonic distortions. Subsequently, achieving fast tracking and strong robustness against dynamic changes of harmonics, simultaneously, seems to be very challenging.

In general, advanced signal processing methods are presented either in time or frequency domain strategies for the

appropriate operation of a DSTATCOM control system. Frequency-domain strategies, such as Discrete Fourier Transform (DFT) [9] and Kalman Filter (KF) [10] generally show a slow time response and cannot track harmonic variations suitably. However, time-domain strategies, like Instantaneous Reactive Power Theory (IRPT) [11] and synchronous reference frame theory (SRFT) [12] show a better dynamic response and have effective compensation performance during different operation cases. Traditionally, Phase Lock Loops (PLL) are used to detect harmonic elements in disrupted power signals. When the voltage is unbalanced or disturbed, PLL can experience delays in phase, leading to slow reactions and potential system failures. Typically, PLL optimization involves balancing quick detection and effective filtration, which is tricky since these methods often struggle with harmonic distortions. Therefore, finding a solution that quickly tracks changes while also being resilient to harmonics is quite a challenge [13,14].

Most of the advanced filtering control methods of DSTATCOM, such as the Least-Mean-Square algorithm (LMS) [15] and the Adaptive Notch Filter (ANF) [16] are accurate and represent appropriate dynamic responses, but introduce slow convergence speed. The authors in [17] propose the Amplitude Adaptive Notch Filter (AANF) strategy as a control system for DSTATCOM to address deficiencies in the ANF control method. This method focuses on extracting reference signals in unbalanced and distorted networks. While successful in generating reference currents, it falls short in providing a rapid and precise response to the system's dynamics. Least Error Square (LES) method is another advanced control algorithm which is identified as an effective control technique for extracting reference sinusoidal components from distorted input signals [18-21]. A fast control scheme relying on the LES filter with a fixed window length was proposed for a Dynamic Voltage Restorer (DVR) control system in [18]. The control strategy estimates the load and source voltages. A novel Software Phase-Locked Loop (SPLL) control algorithm of DVR was proposed [19] based on non-recursive LES filters and realized in the ‘abc’ reference frame and entails a high computational burden. Recursive Least Error Square (RLES) algorithm has been introduced in [22, 23] as a useful fast and robust algorithm because it shows acceptable convergence speed and the harmonic estimated values are updated recursively as soon as signal samples are acquired. RLES can be used in a power system with time-varying loads because these changes create different types of nonlinearity and harmonics with varying amplitudes and phase angles, and harmonic estimated values need to be updated according to the recent signal samples [24]. The accuracy and convergence speed of RLES algorithm are in proportion to the value of forgetting factor. RLES with a fixed forgetting factor fails to properly track time-varying parameters that have large oscillations. So, an adaptive approach should be incorporated in the estimation process to obtain a Variable Forgetting Factor (VFF) [25-27]. The following presents some of the recent papers that have adopted VFF in various applications of electrical engineering. Reference [28] suggests a VFF Recursive Least Squares (RLS) parameter identification approach to precisely determine the parameters used in modelling the lithium battery in real-time. The method utilizes the terminal voltage of the system identification parameter and the measurement terminal voltage to create a window for error calculation. It then dynamically adjusts the forgetting factor based on the error, thereby enhancing the accuracy of system parameter identification through the least square method. The researchers adopted a VFF-RLS method to identify parameters and employed a mixture of covariance square root and noise statistics estimation methods so that the state of charge of batteries are obtained. This approach addressed the issue of dispersion in the unscented Kalman filter and the problem of the error covariance increasing indefinitely during iterative calculations, thereby ensuring accurate estimation of the state of charge [29]. The VFF-RLS method, as proposed in reference [30], incorporates a least square approach with forgetting factors to estimate the electrical parameters of a basic electrical model. A variable-rate forgetting factor was devised for the purpose of parameter identification in time-varying systems using recursive least squares. This factor employs the F-test to make a comparison between the variance of one-step prediction errors in the short and long terms for RLS [31]. Reference [32] proposed a methodology for parameter identification in the variable forgetting factors recursive least squares algorithm using global mean particle swarm optimization. Next, it suggested a global particle swarm optimization search mechanism that focuses on variable time double extended Kalman filtering. The contribution of this paper includes real-time realization of a developed two-layer method relying on the combination of VFF-RLES algorithm as the first layer and an algorithm for reference current extraction for the DSTATCOM control system as the second layer. In the first layer, the weights are updated using a new robust Fuzzy Inference System (FIS)-VFF-RLES algorithm. Therefore, amplitude and phase angle of the fundamental and selected harmonic terms of three-phase voltages and currents are estimated separately from the updated weights without a significant delay. In the second layer, the calculated amplitudes and phase angles help extract the current reference for DSTATCOM controller. Moreover, an Adaptive Hysteresis Band Current (AHBC) controller has been employed to produce switch signals and thus boost the dynamic performance of the DSATATCOM. The proposed control scheme allows DSTATCOM to detect and compensate harmonics with a high accuracy and appropriate convergence speed without losing the robustness against harmonics under linear and nonlinear loads. In the remaining of the paper, Section 2 introduces the DSTATCOM configuration in a three-phase four-wire distribution system. In Section 3, the suggested RLES control scheme and its formulations along with the AHBC controller are described to achieve the appropriate switching signals. In Section 4, the control system is tested to investigate the performance of the control strategy. The control design employed for DSTATCOM under different load conditions in MATLAB software is evaluated in Section 5. Finally, a conclusion is presented in the last section.

2. SYSTEM CONFIGURATION

Fig. 1 shows the layout of a 3ph 4-wire DSTATCOM with a four-leg Voltage Source Converter (VSC). As is observed, eight IGBT-based switches are turned on/off based on the control strategy of DSTATCOM. The system includes a three-phase voltage source with a source resistance (R_s) and a source inductance (L_s). A four-leg VSC with a DC-link

capacitor is connected using interfacing inductors (L_f, L_n) so that high-frequency ripples are cancel out from the source currents. Three legs of the VSC are in connection with the PCC and the remaining leg is in connection with the neutral terminal of the load and source to compensate neutral current. An appropriately fixed capacitor (C_{dc}) is in joined to the DC link of the VSC to damp the transients. An RC filter (R_f, C_f) linked to PCC filters high-frequency ripples from the terminal voltage [33-35]. Various topologies exist for three-phase four-wire DSTATCOM, including the four-leg voltage source converter (VSC), capacitor midpoint VSC, and H Bridge VSC configurations. Among these, the four-leg VSC topology is selected for DSTATCOM applications due to its advantages in simplicity and reliability of control, reduced requirement for solid-state devices, and effective neutral wire current compensation [36].

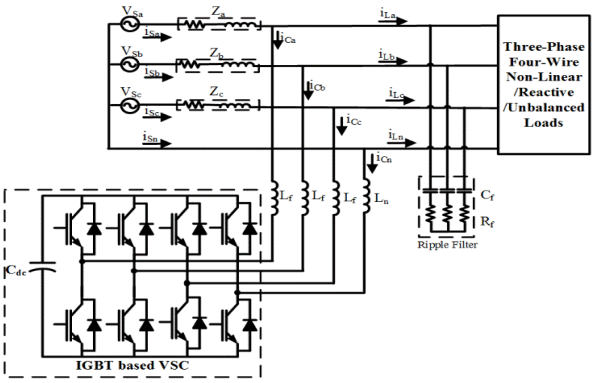

Fig. 1: Connection of a 4-wire DSTATCOM to the distribution network

3. PROPOSED CONTROL SCHEME

3.1. Recursive Least Error Square Algorithm

For power quality purposes, an advanced amplitude, phase and frequency detecting algorithm is required to derive active and reactive components of the input signals. In general, the input signal of control system of DSTATCOM is defined as:

$$y_\alpha(t) = \sum_{i=1}^{n} A_{i\alpha} \sin(i\omega_0 t + \varphi_{i\alpha}) + A_{dc\alpha} e^{-\frac{t}{\tau}}; \alpha = a, b, c \qquad (1)$$

where i represents the order of harmonic components, $A_{i\alpha}$ is the corresponding amplitude of each phase component, $\varphi_{i\alpha}$ is the initial angle, $e^{-\frac{t}{\tau}}$is the dc offset term, and $\omega_0$is the fundamental angular frequency. The main aim of the RLES algorithm here is the estimation of the unknown parameters ($A_{i\alpha}$,$\varphi_{i\alpha}$, $A_{dc\alpha}$). The estimation must be exact and not sensitive to harmonics, inter-harmonics, and noise. In addition, the proposed RLES algorithm is able to operate under small frequency deviations on the supply side because the frequency deviation in the power system is less than 0.2 Hz, whereas the sampling frequency can be about 10 kHz. This makes the algorithm fast and reliable in the case of small frequency deviations.

Considering $y_a(t)$ as the input signal which is sampled at a preselected rate (Δt), then Msamples are obtained as Equation (2). Equation (2) will be written as follows

$$\begin{cases} y_a(t) = A_{1a}\cos\varphi_{1a}\sin(\omega_0 t) + A_{1a}\sin\varphi_{1a}\cos(\omega_0 t) + \sum_{i=2}^{n} A_{ia}\cos\varphi_{ia}\sin(i\omega_0 t) + \sum_{i=2}^{n} A_{ia}\sin\varphi_{ia}\cos(i\omega_0 t) + A_{dc} - \frac{A_{dc}}{\tau}t \\ y_a(t-\Delta t) = A_{1a}\cos\varphi_{1a}\sin\omega_0(t-\Delta t) + A_{1a}\sin\varphi_{1a}\cos\omega_0(t-\Delta t) + \sum_{i=2}^{n} A_{ia}\cos\varphi_{ia}\sin i\,\omega_0(t-\Delta t) \\ + \sum_{i=2}^{n} A_{ia}\sin\varphi_{ia}\cos i\,\omega_0(t-\Delta t) + A_{dc} - \frac{A_{dc}}{\tau}(t-\Delta t) \\ \vdots \\ y_a[t-(M-1)\Delta t] = A_{1a}\cos\varphi_{1a}\sin\omega_0[t-(M-1)\Delta t] + A_{1a}\sin\varphi_{1a}\cos\omega_0[t-(M-1)\Delta t] \\ + \sum_{i=2}^{n} A_{ia}\cos\varphi_{ia}\sin i\,\omega_0[t-(M-1)\Delta t] + \sum_{i=2}^{n} A_{ia}\sin\varphi_{ia}\cos i\,\omega_0(t-\Delta t) \\ + A_{dc} - \frac{A_{dc}}{\tau}[t-(M-1)\Delta t] \end{cases} \qquad (2)$$

$$\begin{aligned} &[Y_a]_{M\times 1} = [A_a]_{M\times 2n+2} \times [X_a]_{2n+2\times 1} \\ &[X_a] = \left[A_{1a}\cos\varphi_{1a} \quad A_{1a}\sin\varphi_{1a} \quad \dots \quad A_{na}\cos\varphi_{na} \quad A_{na}\sin\varphi_{na} \quad A_{dc} \quad \frac{A_{dc}}{\tau}\right] \\ &[Y_a] = [y_a(t) \quad y_a(t-\Delta t) \quad \dots \quad y_a[t-(M-1)\Delta t]^T \\ &[A_a] \\ &= \begin{bmatrix} \sin(\omega_0 t) & \cos(\omega_0 t) & \cdots & \sin n(\omega_0 t) & \cos n(\omega_0 t) & 1 & t \\ \sin\omega_0(t-\Delta t) & \cos\omega_0(t-\Delta t) & \cdots & \sin n\,\omega_0(t-\Delta t) & \cos n\,\omega_0(t-\Delta t) & 1 & t-\Delta t \\ \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \vdots \\ \sin\omega_0[t-(M-1)\Delta t] & \cos\omega_0[t-(M-1)\Delta t] & \cdots & \sin n\,\omega_0[t-(M-1)\Delta t] & \cos n\,\omega_0[t-(M-1)\Delta t] & 1 & t-(M-1)\Delta t \end{bmatrix} \end{aligned} \qquad (3)$$

The solution of (3), based on the least error square method, is calculated by:

$$[X_a] = \left[[A_a]^T \times [A_a]\right]^{-1} \times [A_a]^T \times [Y_a] \quad (4)$$

To implement (4) in a recursive mode and to estimate the desired parameter by RLES algorithm, the following error function should be minimized in each iteration:

$$E(n) = \sum_{i=1}^{n} \{\lambda^{n-i} e^2(i)\} \quad (5)$$

where $\lambda \in (0,1]$ is the forgetting factor which adapts the parameters according to the input signal variations.

According to (5), the updated parameter vector can be found as follows:

$$\hat{A}(k) = \hat{A}(k-1) + \mu(k)e(k) \quad (6)$$

where the error is

$$e(k) = y(k) - \hat{A}^T(k-1)X(k) \quad (7)$$

The gain μ(k) is the covariance of parameter vector as:

$$\mu(k) = R(k-1)X(k)[\lambda + X^T(k)R(k-1)X(k)]^{-1} \quad (8)$$

$$R(k) = \frac{1}{\lambda}[R(k-1) - \mu(k)X^T(k)R(k-1)] \quad (9)$$

Equations (6-9) are estimated by the following initial values:

$\hat{X}(-1) = 0$, $R = \pi_0 I$, where R is the initial covariance matrix, π_0 is a large number, and I is a square identity matrix [22].

Note that π_0 influences the convergence gain; faster convergence can be achieved by choosing a largerπ_0. The convergence speed and tracking capability of RLES algorithm are directly related to the initial values and the forgetting factor (λ). Forgetting factor highly impacts the estimation speed of RLES algorithm and the proper value is chosen considering the convergence speed and tracking capability [25]. A smaller value of λ leads to a faster estimation speed, however, inappropriate tracking capability. On the other hand, a larger value of λ (close to 1) represents an appropriate tracking capability with the reduced convergence speed. Consequently, this problem can be addressed by a time-varying adaptive control method for the selection of forgetting factor during both steady-state and dynamic situations where the system parameters are changed abruptly. Since FIS theory does not rely on the mathematical formulation of the object to be controlled, and is robust than the traditional control methods, a FIS-based VFF (λ) is developed in this paper and an appropriate forgetting factor is chosen by a FIS so that higher convergence rate and lower steady-state oscillation are achieved.

Here, the squared error $e^2(k)$ and its variation $\Delta e^2(k) = |e^2(k) - e^2(k-1)|$ are considered as input variables of the fuzzy logic control system at the kth iteration and $\lambda = FIS[e^2(k), \Delta e^2(k)]$ is considered as the output. Four triangle Membership Functions (MFs), Very Large (VL), Large (L), Medium (M), and Small (S), are selected as the input and output variables (Fig. 2). A set of fuzzy IF–THEN rules are established in Table 1 which come from a combination of a small value of λ during transient conditions (for the improvement of the RLES estimation speed) and a fixed (near to 1) in steady state conditions.

The MFs of the input and output variables are chosen in a way that they are not influenced by the noise of the input signal. In general, MFs of the proposed FIS-VFF is tuned based on the fast transient performance, steady state response, and noise rejection capability. The suggested method allows for the efficient and accurate estimation of frequency components in the observed signal, adapting to changes in frequency both during steady-state and transient circumstances.

Having updated unknown parameter vectors using the proposed algorithm, the amplitude and phase angle of each harmonic component is evaluated as follows:

$$\begin{cases} A_i = \sqrt{(A_i \cos\varphi_i)^2 + (A_i \sin\varphi_i)^2} \\ \varphi = arctan(A_i \sin\varphi_i, A_i \cos\varphi_i) \end{cases} \quad (10)$$

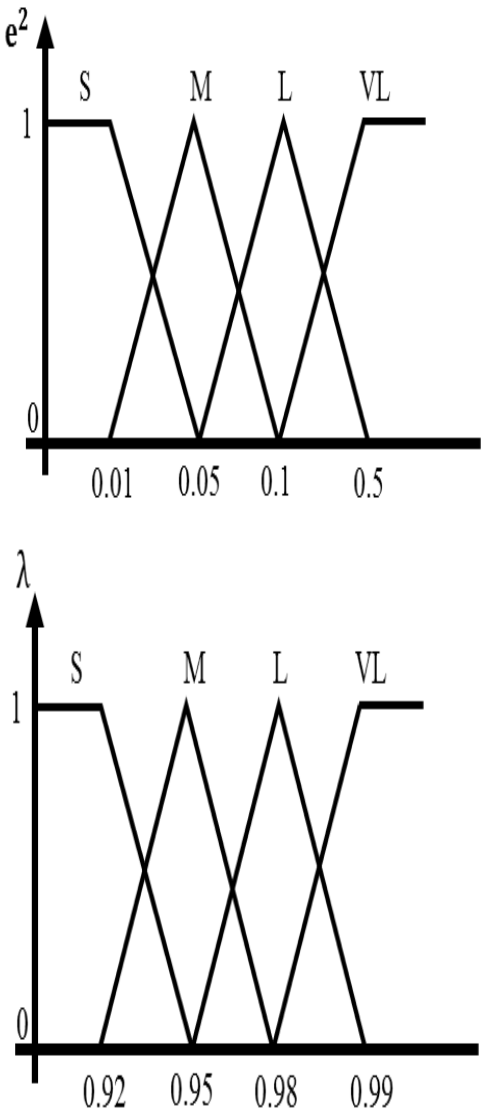

Fig. 2: The MFs of inputs and output

TABLE 1: FUZZY DECISION TABLE

e^2 \ Δe^2	S	M	L	VL
S	VL	VL	VL	L
M	L	L	M	M
L	M	M	S	S
VL	S	S	S	S

The main term of the input signal can be represented as

$$y_1 = A_1 \sin \varphi_1 \tag{11}$$

For simplification of the proposed algorithm, only fundamental, fifth, and seventh harmonic terms are considered in the calculations.

Subsequent harmonic elimination/extraction and subsequent harmonic analysis are both possible with the assistance of this algorithm, which ensures the rapid and accurate extraction of individual harmonics. Furthermore, this structure is insensitive to different load and grid conditions, and does not require any synchronizing tools such as PLL.

3.2. Proposed Compensation Strategy

The inputs to this section are the calculated amplitude and phase angle of the fundamental components of the measured voltage and current which are calculated by the VFF-RLES in section 3.1.

The fundamental component of line current, $i_b(t)$, is divided into active current, $i_{ba}(t)$ and the reactive current, $i_{br}(t)$:

$$i_b(t) = i_{ba}(t) + i_{br}(t) \tag{12}$$

Equation (13) expresses the active and reactive currents of Eq. (12):

$$\begin{cases} i_{ba}(t) = I_m \cos(\varphi_i - \varphi_v).\sin(\varphi_v) \\ i_{br}(t) = I_m \sin(\varphi_i - \varphi_v).\cos(\varphi_v) \end{cases} \tag{13}$$

where $I_m$is the amplitude of $i_b(t)$, φ_i is the total phase angle of $i_b(t)$, and $\varphi_v$represents the total phase angle of the fundamental component of relative phase-to-ground voltage. By re-arranging (13) for three phases:

$$\begin{cases} i_{aa}(t) = [I_{m\,a}\cos(\varphi_{ia}).\cos(\varphi_{va}) + I_{m\,a}\sin(\varphi_{ia}).\sin(\varphi_{va})].\sin(\varphi_{va}) \\ i_{ab}(t) = [I_{m\,b}\cos(\varphi_{ib}).\cos(\varphi_{vb}) + I_{m\,b}\sin(\varphi_{ib}).\sin(\varphi_{vb})].\sin(\varphi_{vb}) \\ i_{ac}(t) = [I_{m\,c}\cos(\varphi_{ic}).\cos(\varphi_{vc}) + I_{m\,c}\sin(\varphi_{ic}).\sin(\varphi_{vc})].\sin(\varphi_{vc}) \end{cases} \tag{14}$$

and:

$$\begin{cases} i_{ra}(t) = [I_{m\,a}\sin(\varphi_{ia}).\cos(\varphi_{va}) - I_{m\,a}\cos(\varphi_{ia}).\sin(\varphi_{va})].\cos(\varphi_{va}) \\ i_{rb}(t) = [I_{m\,b}\sin(\varphi_{ib}).\cos(\varphi_{vb}) - I_{m\,b}\cos(\varphi_{ib}).\sin(\varphi_{vb})].\cos(\varphi_{vb}) \\ i_{rc}(t) = [I_{m\,c}\sin(\varphi_{ic}).\cos(\varphi_{vc}) - I_{m\,c}\cos(\varphi_{ic}).\sin(\varphi_{vc})].\cos(\varphi_{vc}) \end{cases} \tag{15}$$

In addition, the amplitude of phase voltage (V_t), in-phase unit templates (u_{ap}, u_{bp}, u_{cp}), and quadrature unit templates (u_{aq}, u_{bq}, u_{cq}) are evaluated by the fundamental component of PCC voltage driven by the RLES algorithm [37,38]. According to reference [39], the angle φ itself is a function of *t*, but in the article, to avoid lengthening the equations, we only mention it with the symbol (φ).

The proposed RLES algorithm can be incorporated in many operation states of the DSTATCOM, like power factor modification, zero-voltage adjustment, load equilibrium, and current harmonic removal.

3.3. Power Factor Correction (PFC) operation of DSTATCOM

The compensatory method for the PFC operation involves injecting the average active term of the load current, besides the active power term, so that the magnitude of the DC bus voltage is adjusted to the desired magnitude.

The active power term of the load current should have an identical amplitude across all phases. This can be determined using (14) to ensure imbalances are cancelled out from the reference source currents. The mean magnitude of the active term of load currents will be calculated as:

$$I_{ad}(t) = (i_{aa}(t) + i_{ab}(t) + i_{ac}(t))/3 \tag{16}$$

A self-supporting DC bus capacitor is in connection with the DC side of the VSC and its voltage controlled by a PI controller to compensate for active power losses in the DSTATCOM. The output of PI (proportional– integral) controller of the dc bus voltage of the DSTATCOM is taken as the loss term of the current (I_{loss}).

The magnitude of the reference source active current is determined via summing the fundamental active power term of the load currents with the current's loss term:

$$I_{as}(t) = I_{ad}(t) + I_{loss} \tag{17}$$

The magnitude of reference source currents is multiplied by in-phase unit templates to produce the instantaneous reference source currents:

$$i^*_{sap} = I_{as} * u_{ap}, i^*_{sbp} = I_{bs} * u_{bp}, i^*_{scp} = I_{cs} * u_{cp} \tag{18}$$

These generated reference active source current components are in-phase with the phase voltages for power factor correction operation. Thereby, the reactive power demand of the load is fully fed via the DSTATCOM.

3.4. Zero Voltage Regulation (ZVR) operation of DSTATCOM

The compensatory approach for the ZVR operation assumes that the source provides equivalent active current components in addition to the total of reactive current components, which is evaluated by (15), and the component found from a PI controller (I_{vt}) utilized for adjusting the voltage at PCC. The magnitude of AC terminal voltage (V_t) at the PCC's voltage is regulated to the reference voltage (V_t^*) by the PI controller.

The average amplitude of the reactive power term of the load currents will be obtained as:

$$I_{rq}(t) = (i_{ra}(t) + i_{rb}(t) + i_{rc}(t))/3 \tag{19}$$

In addition, the output of the PI controller of the PCC voltage is the reactive power term used for regulating the PCC voltage at the load terminals.

The calculation for determining the total reactive current term of the reference source currents involves deducting the average fundamental reactive current term from the reactive power component:

$$I_{rs}(t) = -I_{rq}(t) + I_{vt}(t) \quad (20)$$

The reference reactive source current components which are in quadrature with the three phase voltages are estimated as:

$$i^*_{saq} = I_{rs} * u_{aq}, i^*_{sbq} = I_{rs} * u_{bq}, i^*_{scq} = I_{rs} * u_{cq} \quad (21)$$

Finally, the reference source currents are expressed by summing the active and reactive reference terms of the source currents for each of the three phases:

$$i^*_{sa} = i^*_{sap} + i^*_{saq}, i^*_{sb} = i^*_{sbp} + i^*_{sbq}, i^*_{sc} = i^*_{scp} + i^*_{scq} \quad (22)$$

The reference current for the source neutral current is assumed zero:

$$i^*_{sn} = 0 \quad (23)$$

A comparison is made between the derived reference source currents ($i^*_{sa}, i^*_{sb}, i^*_{sc}$) and the corresponding measured source currents (i_{sa}, i_{sb}, i_{sc}), where the error is applied to the current controller to produce the gate signals for the DSTATCOM switches.

Fig. 3 shows the compensation strategy.

3.5. Switching Algorithm

Fig. 2 compares the measured source currents (i_{sa}, i_{sb}, i_{sc}) and the estimated reference source currents ($i^*_{sa}, i^*_{sb}, i^*_{sc}$), where the error signals are applied to the adaptive hysteresis band current controller to produce the gating signals for insulated gate bipolar transistor (IGBT) switches of the VSC-based DSTATCOM.

The hysteresis band current control technology has been extensively adopted for active power filters. The hysteresis band current control exhibits inherent stability, rapid response, and high precision. However, the standard hysteresis technique also has various drawbacks, including an asymmetrical switching frequency that results in acoustic noise and additional switching losses. Narrow bandwidth results in a fast and fairly tracking of currents, while significantly raising the switching frequency. A wide bandwidth also does not offer an accurate tracking and may cause instability. To avoid these drawbacks, a system is equipped with an adjustable hysteresis band. This enables the hysteresis band to be adjusted based on the system characteristics so that a nearly constant switching frequency is preserved.

For almost constant switching frequency, the hysteresis band will be:

$$HB = \frac{V_{dc}}{8.f_c.L_f}[1 - \frac{4L^2}{V_{dc}^2}(\frac{V_s(t)}{L_f} + m)^2] \quad (24)$$

where f_c is the modulation frequency and $m = \frac{di^*_{sa}}{dt}$ shows the slope of command current wave. Adaptive hysteresis band changes the hysteresis bandwidth (HB) based on the modulation frequency, supply voltage, dc capacitor voltage, and slope of the source reference current. Moreover, modulation can be applied to it to manage the switching scheme of the inverter [40, 41].

Power circuit parameters including DC bus voltage, AC inductors, and the VSC in three-phase four-leg DSTATCOM are given in Appendix and selected based on [41-44] with respect to the system configuration.

4. Performance Evaluation

By means of computer simulations carried out inside the MATLAB/Simulink environment, this part evaluates the efficacy of the control method suggested for DSTATCOM. In this section, the tracking capability and harmonic removal potential of the suggested RLES are examined. Additionally, the performance of the entire system with regard to load equilibrium, harmonic removal, neutral current compensation, and power factor modification are discussed in Section 5.

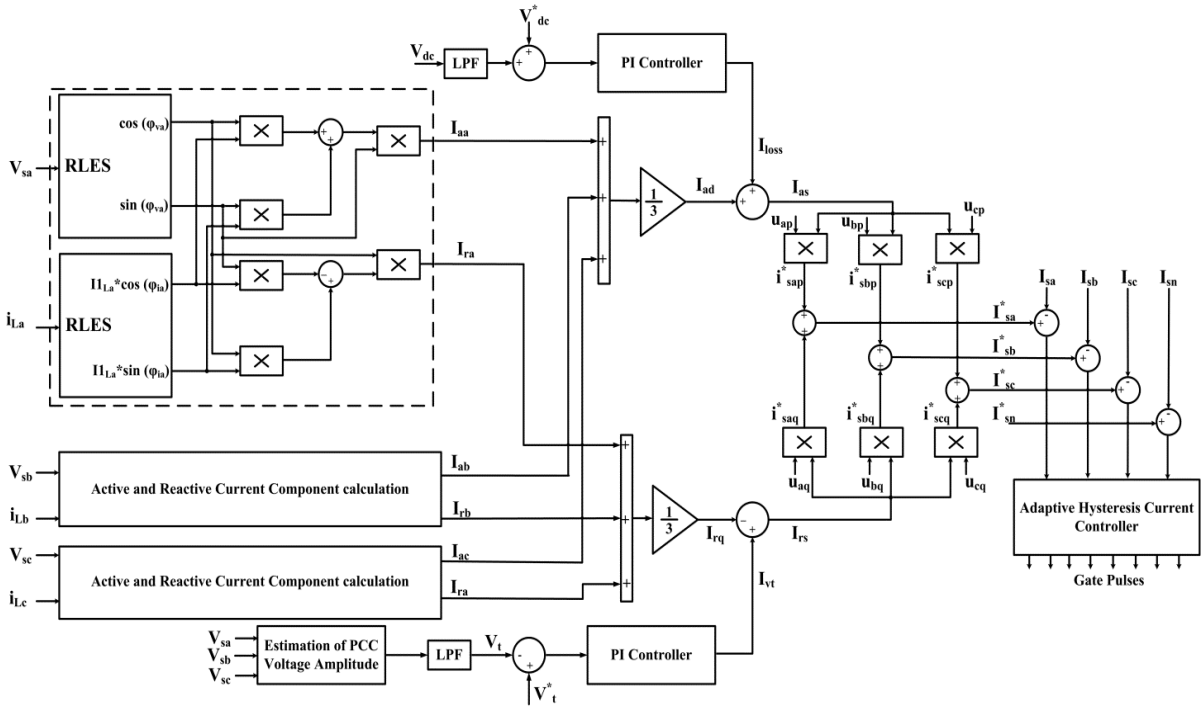

Fig. 3: Schematic diagram of the compensation strategy

4.1. Initial performance

The input signal of the RLES is assumed as Eq. (25):

$$y(t) = sin(\omega_0 t + \varphi_1) + 0.2\, sin(5\omega_0 t + \varphi_5) + 0.3\, sin(7\omega_0 t + \varphi_7) + 0.3\, sin(30\omega_0 t + \varphi_{30}) \quad (25)$$

where $\omega_0 = 100\pi$ rad/s and the initial phase angles φ_i's are chosen in a random process in the range of 0 and 2π rad. The system's response to the input signal of (25), i.e., four extracted signals including the fundamental, the fifth, and the seventh harmonic terms, are shown in Fig. 4.

4.2. Harmonic Detection Capability

In this section, the proposed structure is used to track and extract harmonic components of an input signal as follows:

$$y(t) = sin(\omega_0 t + \varphi_1) + 0.3\, sin(5\omega_0 t + \varphi_5) + 0.2\, sin(7\omega_0 t + \varphi_7) \quad (26)$$

A step change of (−0.2 pu) in the amplitude of the fundamental and the 5th harmonic component, and (+ 0.2 pu) in the amplitude of the 7th harmonic at t = 0.2 s with comparison between fixed forgetting factor RLES and the proposed RLES algorithms are considered. As it is shown in Figs. 5 and 6, both schemes track the step changes of the fundamental, the 5th and the 7th components amplitudes and phase angles, and compared to the fixed forgetting factor RLES scheme, proposed RLES performs satisfactorily with regard to tracking the changes of amplitude of the fundamental component of the input signal during transient condition.

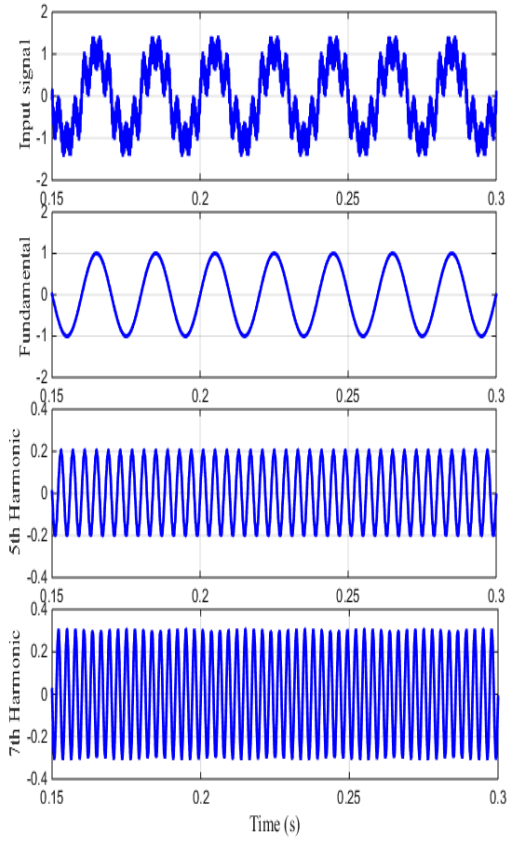

Fig. 4: The input signal and its fundamental, 5th and 7th harmonic components of the input signal using proposed RLES

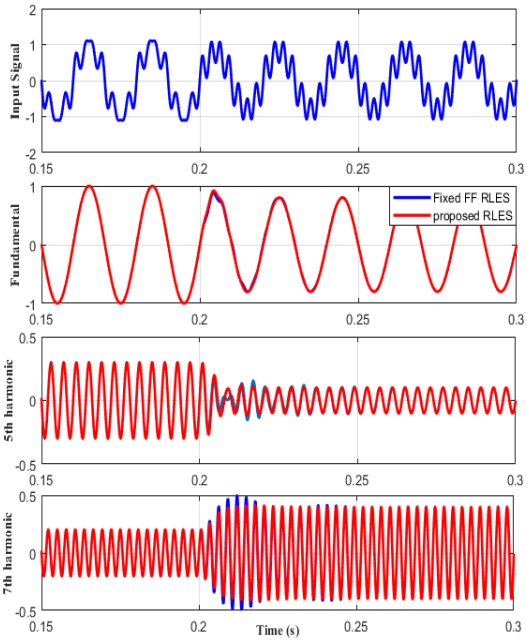

Fig. 5: Amplitude tracking changes of the fundamental, 5th and 7th harmonic components

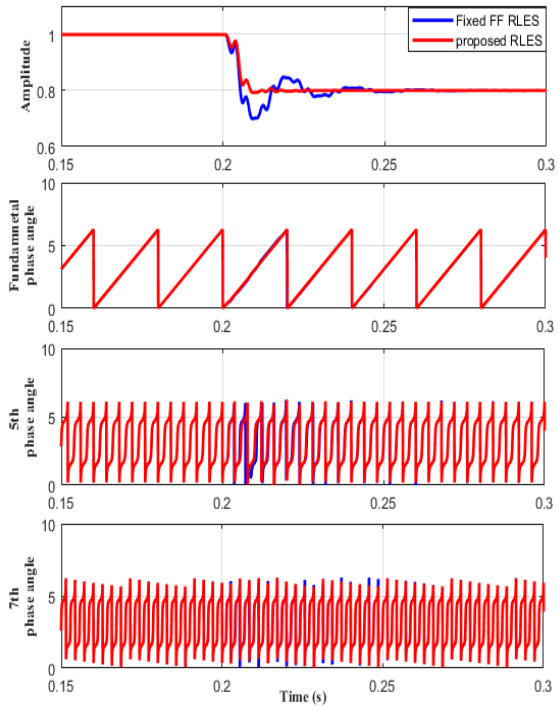

Fig. 6: Amplitude and phase tracking changes of fundamnetal, fifth and seventh harmonic terms

5. Analytical Studies and Discussion

To modify power factor correction, regulate voltage, remove harmonic terms, balance the load, and compensate neutral current, the performance of the three-phase four-leg DSTATCOM is demonstrated by utilizing the proposed RLES-based control design. In this study, the model is examined in four distinct scenarios, each of which involves linear and non-linear load circumstances. Four different worst possible conditions are discussed in this section.

Voltage source is unbalanced and distorted and unbalanced linear and non-linear loads are presented to survey the performance DSTATCOM with RLES-based control algorithm.

5.1. PFC operation of DSTATCOM during linear lagging power factor load (Case A)

The power factor correction and load balancing operation of the suggested RLES-based control algorithm of the four-leg DSTATCOM are described in this subsection. At t= 0.4 and t= 0.5 s, phases 'A' and 'B' are disconnected, respectively, and at t= 0.7 s and t= 0.8 s, phases 'A' and 'B' are reconnected. Fig. 7 displays the three-phase source voltage (v_{source}), load currents (i_{load}), compensating currents ($i_{DSTATCOM}$), source currents (i_{source}), and DC bus voltage (V_{dc}). It is observed that after $t = 0.4$ s, DSTATCOM injects currents in order to maintain three phase source currents balanced in spite of unbalancing in the load currents. As a result, three phase source currents appear balanced and DC bus voltage is fixed at almost its reference value even in unbalanced conditions. It shows the function of DSTATCOM for load balancing and also observed the fast action of RLES during sudden load injection. Fast action of RLES algorithm can be seen at a time of load injection in the estimation of reference supply current with other signals. Just at the time of load injection, nature of DSTATCOM current is changed quickly which validates the fast action of this proposed control method. These results show satisfactory performance of the proposed control algorithm used in DSTATCOM for reactive power compensation and harmonics suppression under linear and nonlinear loads respectively.

Figs. 8 and 9 show reactive power compensation performance and the neutral current elimination of the proposed control method, respectively. Simultaneously, DSTATCOM compensates for the reactive current of the load, modifies power factor, and removes zero-sequence current terms. It is observed that although the power factor of the load is about 0.8, the source side power factor is maintained equal to unit and the supply voltages and currents are in-phase. DSTATCOM also injects compensation currents so that the source-side neutral current is maintained near zero.

5.2. ZVR operation of DSTATCOM during linear lagging power factor load (Case B)

Fig. 10 shows the ZVR performance of DSTATCOM for linear unbalanced load operation. In this mode, the magnitude of load terminal voltage is adjusted to the desired value. The performance indices are as load currents (i_{load}), compensator currents ($i_{DSTATCOM}$), source currents (i_{source}), magnitude of voltages at the PCC (V_{PCC}), and DC-link voltage (V_{dc}) when time-varying linear loads are present. This figure shows the balanced source currents at PCC and its smooth change over when load currents are not balanced. It means that during load dynamics, the reference source currents generated through control algorithm are exactly follow the sensed source currents. It shows almost balanced supply currents when load currents are unbalanced. These results show satisfactory performance of the RLES used in DSTATCOM for load balancing under non-linear loads in voltage regulation mode. The source current is made balanced and the PCC voltage range and the DC-bus voltage remain almost close to the reference values. The power factor on supply side is leading as the terminal voltage is regulated by the DSTATCOM. It is observed that PCC voltage is regulated near to rated value. In this mode, supply currents are slightly leading with respective voltages because extra leading reactive power is required to regulate PCC voltages. These results demonstrate satisfactory performance of the control algorithm used for PCC voltage regulation with harmonics elimination in DSTATCOM under nonlinear load.

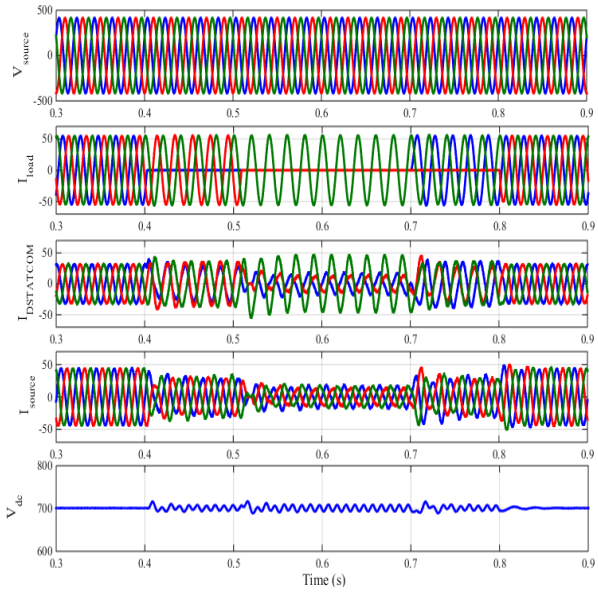

Fig. 7: DSTATCOM performance for load current balancing in case A

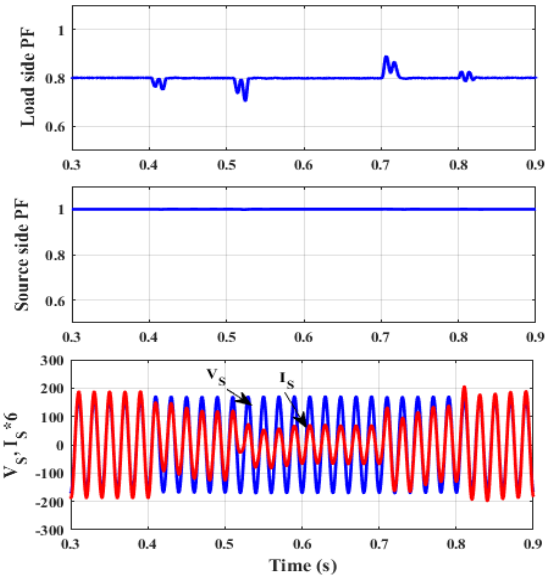

Fig. 8: DSTATCOM performance for power factor correction in case A

5.3. PFC operation of DSTATCOM during nonlinear load (Case C)

Fig. 11 illustrates the dynamic operation of the suggested control algorithm for DSTATCOM in the PFC operation during non-linear load condition. The load unbalancing situation is realized by disconnecting phases 'A' (during t = 0.4s to 0.7s) and 'B' loads (during t = 0.5s to 0.8s). DSTATCOM injects compensating currents s that the three-phase source currents are balanced and without harmonics. It demonstrates sinusoidal balanced source currents, despite load currents being unbalanced and distorted. Also, it demonstrates the fast characteristics of the suggested control design in the case the two phases of the load are disconnected. These simulation findings confirm the functionalities of DSTATCOM for power factor modification and load balancing, as well as harmonic correction under varied non-linear loads. They also demonstrate that the control algorithm is capable of performing its tasks effectively. The operation indicators for this case are three phase load currents (i_{load}), compensating currents ($i_{DSTATCOM}$), balanced sinusoidal source currents (i_{source}), and DC link voltage (V_{dc}). It is shown that the dc bus voltage (V_{dc}) is maintained to the reference dc bus voltage of 700 V. For a better observation of the DSTATCOM performance of harmonic compensation in case C, the THD% of the load current, and the source current in phase 'A' for the PFC operation of DSTATCOM can be observed in Figs. 12 and 13, respectively. The source current THD is 3.27% while the THD% of phase 'A' load current is 24.27 %. Furthermore, by checking phase 'A' PCC voltage (V_{sa}) and the corresponding source current (i_{sa}) in Fig. 14, one can see that both are in-phase and the source power factor is fixed to 1, thus proving the suitable PFC operation mode of DSTATCOM under load dynamics.

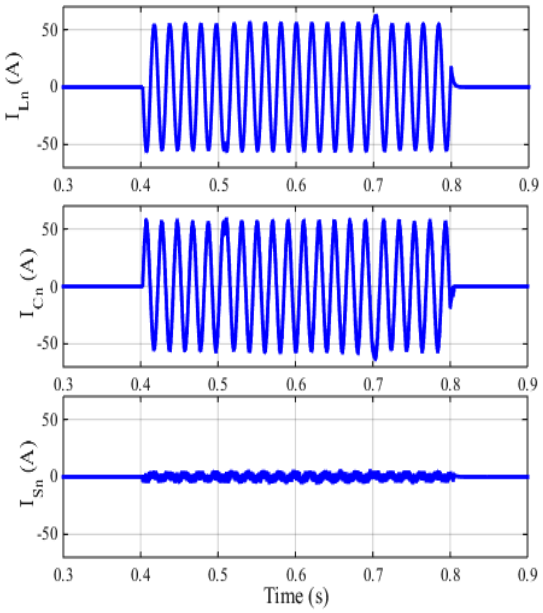

Fig. 9: DSTATCOM performance for neutral current compensation in case A

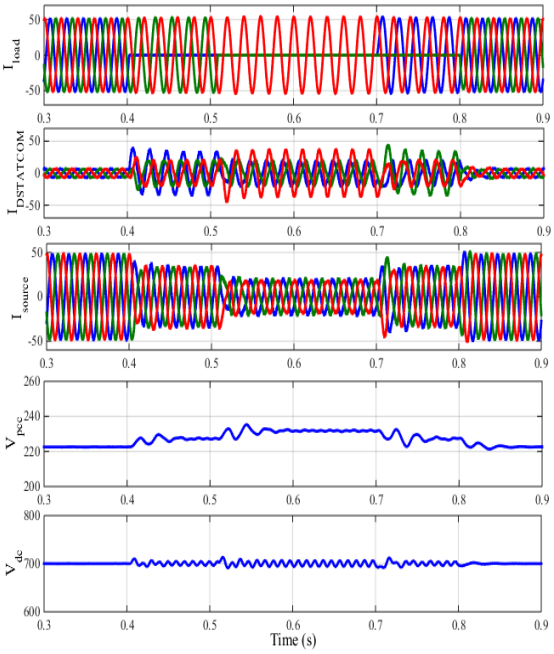

Fig. 10: DSTATCOM performance for load equilibrium and zero-voltage adjustment in Case B

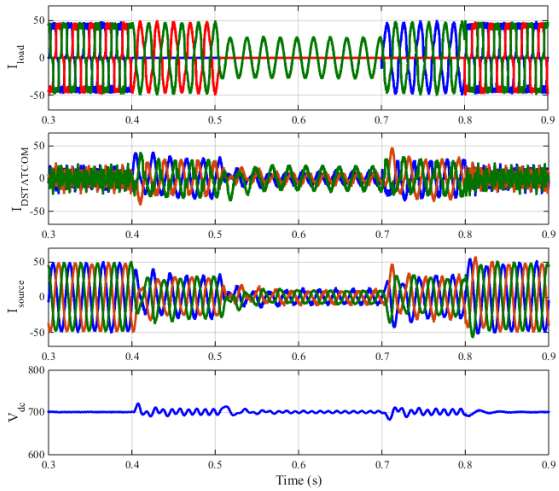

Fig. 11: DSTATCOM performance for load current balancing and harmonic compensation in case C

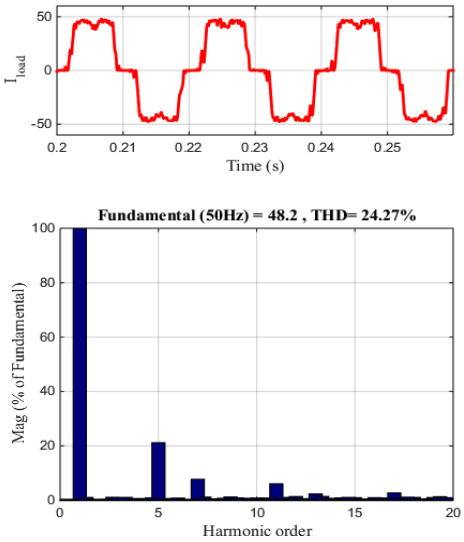

Fig. 12: THD% of load current in case C

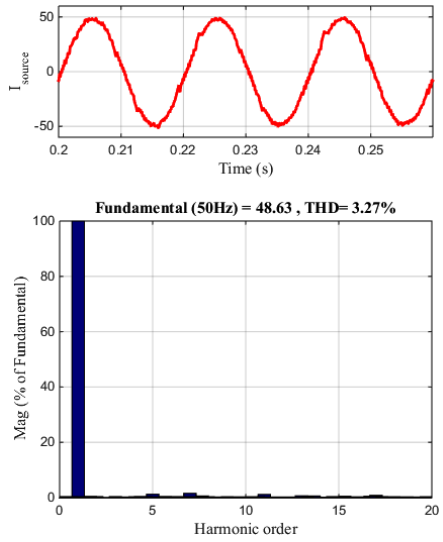

Fig. 13: THD% of source current in case C

5.4. ZVR operation of DSTATCOM for nonlinear loads (Case D)

Fig. 15 illustrates the dynamic behaviour of the proposed control theory for four-leg VSC based DSTATCOM employed for load balancing, harmonics current elimination, voltage regulation, and neutral current compensation under non-linear load condition. In the ZVR mode, the operation indicators for dynamic performance are load currents (i_{load}), compensator currents ($i_{DSTATCOM}$), source currents (i_{source}), magnitude of PCC voltage (V_{PCC}), and DC-link voltage (V_{dc}). In this case, source currents become balanced and perfectly sinusoidal. It also shows the appropriate performance of DSTATCOM in neutral current compensation. Furthermore, the magnitude of PCC voltage (V_{PCC}) is adjusted to the reference value by supplying reactive power. These results show satisfactory performance of the proposed control algorithm in four-leg DSTATCOM for its multi-functions such as reactive power compensation, harmonics suppression and neutral current compensation under non-linear loads, respectively.

In this paper, one of the powerful and famous optimization algorithms (e.g. Genetic Algorithm) is applied for precise calculation of optimized coefficients (PI gains) and accurate comparison between PI and Fuzzy controllers. In the first step individuals with random chromosomes are generated that set up the initial population. In this step, initial population of 20, 50 100 are used and compared which the solutions are similar. Furthermore, integral time absolute error (ITAE) criterion is employed to find the optimum PI controller gains. The new PI coefficients, calculated in these ways, are implemented in controller to demonstrate the improvement of convergence speed, reduction of error, the overshoot in capacitor voltage and other circuit parameters.

Fig. 16 depicts the DSTATCOM operation for neutral current compensation in ZVR operation. Load neutral current (i_{Ln}), injected DSTATCOM neutral current (i_{Cn}), and source neutral current (i_{Sn}) are depicted in this figure, which shows the appropriate operation of DSTATCOM in neutral current compensation.

Fig. 17 demonstrates the harmonics spectra and waveforms of phase 'A' source current. THDs % of phase 'A' at source current is equal to 1.98%.

The waveforms demonstrate that even following the compensation, the mains currents remain sinusoidal. The results demonstrate the effective performance of the suggested algorithm as a control method for load balancing, reactive power compensation, and harmonic removal of both linear and nonlinear loads.

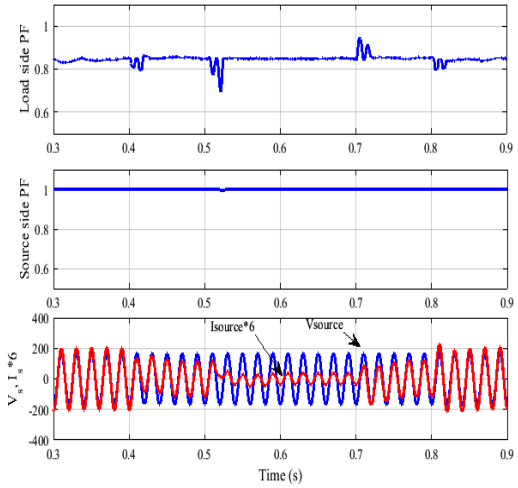

Fig. 14: DSTATCOM performance for power factor correction in case C

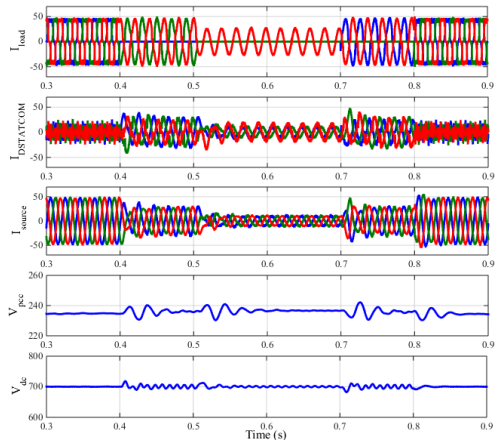

Fig. 15: DSTATCOM performance for load balancing, harmonic compensation and zero voltage regulation in case D

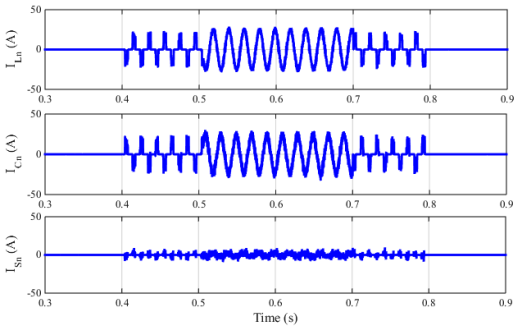

Fig. 16: DSTATCOM performance for neutral current compensation in case D

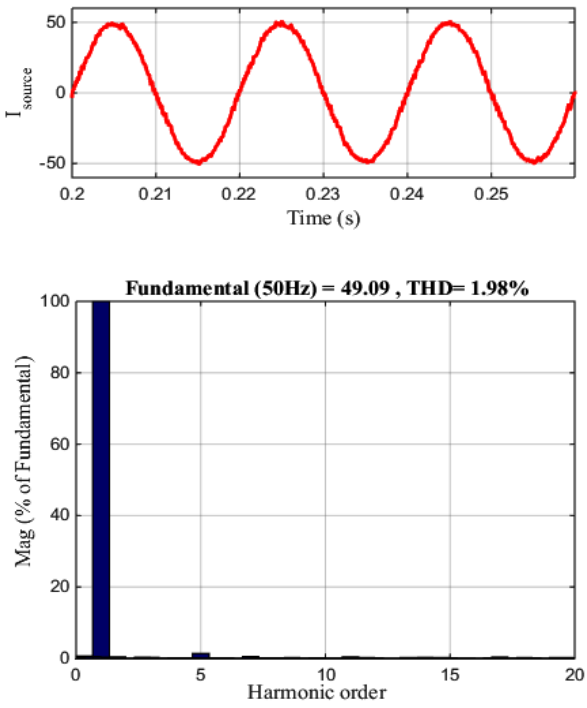

Fig. 17: THD% of source current in case D

A comparison in terms of THD% between RLES and LES algorithm is done in for case D. It can be seen from Table 2 that RLES algorithm perform more successful than LES algorithm during transients.

Table 2: comparison of RLES and LES algorithms in terms of THD%

Three phases	THD% of source currents ($0.4 < t < 0.5$)	
	RLES algorithm	LES algorithm
Phase A	4.21%	4.72%
Phase B	3.4%	4.43%
Phase C	3.48%	4.15%

To survey the load and source currents and comparison of using different controllers in terms of harmonic components and THD% value, harmonic measurements are performed based on the IEEE Std. 519-2014 [45] by measuring harmonics in a considerably short period. The assessment of very short time harmonics is performed during a 3-second period by aggregating 15 successive 10-cycle windows for power systems operating at a frequency of 50 Hz. The aggregation of individual frequency components is performed by applying *rms* calculation, as depicted in Equation (27). In this equation, *F* represents the rms value of voltage or current, *n* indicates the harmonic order, and *i* shows a basic counter. The subscript "*vs*" is utilized to indicate "very short" [43]. Table 3 shows the results for harmonic orders up to 50. The THD percentage values are found based on these harmonic orders.

$$F_{n,vs} = \sqrt{\frac{1}{15}\sum_{i=1}^{15} F_{n,i}^2} \qquad (27)$$

Table 3 illustrates the three-phase load currents and source currents with a comparison of the conventional hysteresis current controller, adaptive hysteresis band current controller, fixed forgetting factor RLES control strategy and the suggested RLES control strategy. According to the findings, the DSTATCOM with the presented RLES control strategy along with an adaptive hysteresis band current controller outperforms their counterparts when THD% values are considered.

6. CONCLUSION

The research presented a novel control scheme for DSTATCOM integration, focusing on a two-layer approach for enhanced power system performance. The first layer introduced a Recursive Least Error Square (RLES) algorithm, refined by a newly designed Fuzzy Inference System-Variable Forgetting Factor (FIS-VFF). This layer efficiently estimated fundamental and select harmonic components of three-phase voltages and currents. The second layer utilized these estimations to derive reference source currents for a three-phase four-wire DSTATCOM system. The contributions are significant for several reasons. The proposed scheme exhibited exceptional speed and accuracy in response to dynamic changes in power systems, confirming its suitability for real-world applications. Through simulation, the THD% in supply current was significantly reduced, aligning with IEEE-519 standards, thereby showcasing the system's efficacy in improving power quality. The control strategy demonstrated robust performance, effectively handling various types of power system pollution. This attribute is critical for ensuring system stability and reliability under fluctuating conditions. Incorporation of an adaptive hysteresis band current controller for generating VSC switch gate signals significantly improved the DSTATCOM's dynamic response. This aspect of the design was pivotal in achieving optimal power factor compensation, harmonic balance, and neutral current management. In scenarios involving linear and non-linear loads, the DSTATCOM, governed by the proposed control scheme, adeptly compensated for reactive power and balanced loads, illustrating the system's versatility. The novel FIS-VFF RLES algorithm outperformed conventional methods in accurately tracking and compensating for harmonics, underscoring the advanced capability of the proposed solution. In conclusion, this research successfully demonstrates a comprehensive and innovative approach to DSTATCOM control, offering significant improvements in power quality management. The findings underscore the potential of the proposed scheme to serve as a robust solution for contemporary and future power system challenges.

Table 3: The harmonic measurements result for load a source current.

harmonics measurement in a very short period based on the IEEE Std 519-2014																
Harmonic order	**Load current**			**Source current**												
				The proposed variable forgetting factor RLES						**Fixed forgetting factor RLES**						
				Conventional Hysteresis controller			**Adaptive Hysteresis controller**			**Conventional Hysteresis controller**			**Adaptive Hysteresis controller**			
	Phase A	**Phase B**	**Phase C**	**Phase A**	**Phase B**	**Phase C**	**Phase A**	**Phase B**	**Phase C**	**Phase A**	**Phase B**	**Phase C**	**Phase A**	**Phase B**	**Phase C**	
1	100.00	100.00	100.00	100.00	100.00	100.00	100.00	100.00	100.00	100.00	100.00	100.00	100.00	100.00	100.00	
2	0.11	0.12	0.16	0.09	0.06	0.04	0.62	0.50	0.39	0.08	0.10	0.09	0.55	0.50	0.80	
3	0.16	0.06	0.15	0.02	0.07	0.03	0.02	0.03	0.08	0.16	0.02	0.08	0.04	0.06	0.02	
4	0.12	0.14	0.23	0.03	0.06	0.07	0.14	0.12	0.20	0.05	0.06	0.14	0.26	0.16	0.16	
5	20.75	20.72	20.61	1.19	1.22	1.16	0.68	0.72	0.69	1.21	1.22	1.25	0.63	0.68	0.78	
6	0.17	0.23	0.21	0.04	0.04	0.11	0.03	0.07	0.02	0.03	0.06	0.03	0.06	0.05	0.05	
7	8.65	8.53	8.69	0.56	0.59	0.63	0.36	0.38	0.38	0.60	0.63	0.60	0.34	0.60	0.39	
8	0.08	0.14	0.14	0.07	0.13	0.13	0.21	0.20	0.14	0.02	0.07	0.08	0.13	0.22	0.19	
9	0.23	0.06	0.20	0.06	0.03	0.05	0.04	0.05	0.02	0.11	0.05	0.08	0.03	0.03	0.04	
10	0.21	0.19	0.28	0.06	0.04	0.07	0.12	0.17	0.22	0.02	0.09	0.03	0.25	0.15	0.18	
11	6.11	6.19	6.00	0.63	0.57	0.55	0.65	0.64	0.70	0.63	0.63	0.65	0.74	0.77	0.61	
12	0.18	0.21	0.25	0.05	0.03	0.12	0.01	0.08	0.09	0.05	0.07	0.03	0.09	0.04	0.04	
13	3.40	3.21	3.42	0.11	0.15	0.09	0.07	0.07	0.15	0.10	0.13	0.17	0.11	0.20	0.09	
14	0.23	0.17	0.06	0.05	0.03	0.05	0.12	0.13	0.05	0.04	0.09	0.02	0.06	0.08	0.14	
15	0.12	0.14	0.16	0.04	0.09	0.03	0.04	0.03	0.08	0.07	0.02	0.08	0.04	0.05	0.05	
16	0.25	0.16	0.26	0.06	0.15	0.04	0.05	0.07	0.09	0.06	0.07	0.12	0.12	0.03	0.09	
17	2.88	3.00	2.80	0.48	0.48	0.44	0.49	0.49	0.53	0.55	0.54	0.52	0.56	0.52	0.49	
18	0.13	0.13	0.26	0.06	0.04	0.06	0.08	0.09	0.09	0.04	0.03	0.07	0.07	0.07	0.05	
19	1.58	1.49	1.54	0.14	0.14	0.12	0.13	0.07	0.05	0.11	0.13	0.14	0.12	0.11	0.08	
20	0.24	0.09	0.18	0.05	0.02	0.06	0.18	0.17	0.08	0.04	0.03	0.04	0.09	0.11	0.11	
21	0.16	0.11	0.08	0.05	0.13	0.03	0.05	0.04	0.03	0.05	0.07	0.07	0.03	0.01	0.08	
22	0.23	0.07	0.18	0.06	0.07	0.05	0.11	0.07	0.14	0.10	0.03	0.05	0.18	0.12	0.13	
23	1.63	1.56	1.45	0.51	0.46	0.48	0.39	0.36	0.48	0.47	0.49	0.55	0.40	0.43	0.36	
24	0.06	0.20	0.18	0.04	0.03	0.04	0.06	0.02	0.10	0.07	0.07	0.12	0.08	0.07	0.03	
25	1.11	1.22	1.13	0.22	0.23	0.26	0.23	0.19	0.21	0.24	0.26	0.27	0.34	0.21	0.26	
26	0.08	0.16	0.13	0.04	0.01	0.02	0.16	0.09	0.03	0.04	0.05	0.03	0.15	0.21	0.13	
27	0.23	0.10	0.14	0.10	0.12	0.09	0.05	0.02	0.08	0.17	0.04	0.04	0.09	0.12	0.05	
28	0.13	0.13	0.11	0.03	0.03	0.07	0.14	0.07	0.16	0.04	0.08	0.06	0.19	0.13	0.17	
29	1.05	0.80	0.70	0.28	0.30	0.29	0.26	0.35	0.24	0.26	0.22	0.30	0.20	0.31	0.24	
30	0.07	0.09	0.05	0.06	0.03	0.04	0.02	0.01	0.09	0.02	0.05	0.03	0.06	0.12	0.02	
31	0.36	0.45	0.44	0.20	0.21	0.26	0.08	0.09	0.17	0.23	0.22	0.17	0.24	0.11	0.07	
32	0.11	0.13	0.08	0.05	0.06	0.06	0.06	0.06	0.05	0.03	0.05	0.06	0.05	0.03	0.10	
33	0.30	0.09	0.24	0.10	0.07	0.08	0.06	0.06	0.05	0.04	0.04	0.09	0.05	0.03	0.03	
34	0.12	0.14	0.08	0.06	0.07	0.04	0.12	0.09	0.04	0.03	0.07	0.02	0.12	0.08	0.17	
35	0.32	0.15	0.34	0.17	0.11	0.13	0.20	0.21	0.18	0.11	0.18	0.18	0.14	0.15	0.17	
36	0.07	0.06	0.11	0.03	0.09	0.03	0.09	0.08	0.10	0.03	0.03	0.09	0.07	0.08	0.06	
37	0.64	0.63	0.70	0.22	0.16	0.19	0.13	0.16	0.18	0.17	0.17	0.16	0.17	0.07	0.16	
38	0.05	0.06	0.07	0.02	0.03	0.06	0.04	0.03	0.09	0.02	0.06	0.02	0.07	0.03	0.02	
39	0.14	0.03	0.15	0.04	0.06	0.05	0.05	0.05	0.07	0.12	0.04	0.06	0.04	0.09	0.08	
40	0.04	0.07	0.08	0.03	0.08	0.07	0.04	0.04	0.08	0.05	0.05	0.04	0.06	0.03	0.07	
41	0.30	0.24	0.30	0.15	0.13	0.14	0.10	0.16	0.10	0.13	0.09	0.10	0.07	0.12	0.14	
42	0.05	0.06	0.04	0.03	0.04	0.01	0.03	0.12	0.09	0.04	0.03	0.01	0.10	0.04	0.09	
43	0.36	0.28	0.34	0.08	0.12	0.02	0.14	0.16	0.13	0.12	0.07	0.06	0.07	0.05	0.09	
44	0.06	0.05	0.10	0.02	0.05	0.06	0.12	0.13	0.09	0.01	0.06	0.05	0.05	0.05	0.04	
45	0.03	0.05	0.05	0.02	0.04	0.04	0.04	0.08	0.09	0.06	0.02	0.04	0.06	0.06	0.05	
46	0.04	0.17	0.18	0.03	0.02	0.08	0.08	0.05	0.10	0.06	0.10	0.04	0.08	0.04	0.12	
47	0.09	0.18	0.22	0.07	0.11	0.07	0.15	0.11	0.19	0.11	0.11	0.14	0.13	0.10	0.07	
48	0.08	0.04	0.04	0.06	0.04	0.02	0.05	0.06	0.11	0.05	0.06	0.03	0.02	0.08	0.06	
49	0.09	0.13	0.16	0.04	0.11	0.06	0.10	0.11	0.15	0.05	0.05	0.05	0.17	0.04	0.11	
50	0.07	0.06	0.05	0.03	0.05	0.02	0.12	0.04	0.09	0.06	0.04	0.06	0.03	0.08	0.09	
THD%	23.91	23.83	23.75	1.73	1.75	1.70	1.53	1.50	1.55	1.79	1.79	1.84	1.60	1.63	1.64	

Appendix: System Parameters

Source Voltage: 415 V
Frequency: 50 Hz
Source resistance: 0.01 Ohm
Source Inductance: 2 mH
Linear Load: 20 KVA, PF= 0.8 lag
Non-linear Load: A three single-phase bridge rectifier with an R-L Load
$R = 9\ Ohm$, $L = 1\ mH$
Ripple filter: $R_f = 5\ \Omega$, $C_f = 5.25\ \mu F$
Interfacing inductor: $L_f = 3.5\ mH$ $L_n = 3.5\ mH$
DC bus capacitance of DSTATCOM: 2000 μF
DC bus voltage of DSTATCOM: 700 V
DC voltage PI controller: $K_{pd} = 1.65$, $K_{id} = 0.22$
PCC voltage PI controller: $K_{pq} = 2$, $K_{iq} = 0.2$

CREDIT AUTHORSHIP CONTRIBUTION STATEMENT

Arash Rohani: Conceptualization, Data curation, Formal analysis, Funding acquisition, Investigation, Methodology, Resources, Software, Validation, Roles/Writing - original draft, Writing - review & editing. **Javad Ebrahimi**: Conceptualization, Formal analysis, Methodology, Validation, Roles/Writing - original draft. **Shirin Besati**: Conceptualization, Investigation, Methodology, Resources, Roles/Writing - original draft, Writing - review & editing.

DECLARATION OF COMPETING INTEREST

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper. The ethical issues; including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, redundancy has been completely observed by the authors.

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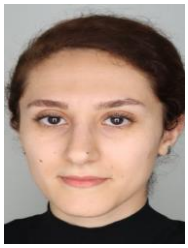

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