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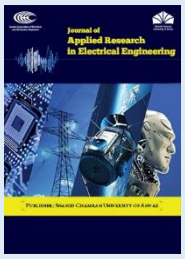

Research Article

A New Topological Method for Output Voltage Clamping of Immittance-based Constant Current Load Resonant Converters

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Abstract - In this paper a new improved diode-based circuit is introduced for output voltage limiting of immittance-based constant current Load Resonant Converters (LRCs). The proposed Diode-based Voltage-Limiter (DVL) is very reliable and simple, and also has minimum number of components. Moreover, limiting values are flexible and can be varied according to the design requirements. All of the positive characteristics of the LRC operation are preserved in this technique such as Zero Voltage Switching (ZVS) of the inverter switches and Zero Current Switching (ZCS) of the rectifier diodes. A 150W converter with 300kHz switching frequency is considered as a sample prototype. The circuit simulation is presented based on the real model of the semiconductor devices in the OrCAD environments to have maximum accordance with the real conditions. Simulation results demonstrate an accurate clamping ability of the output voltage for overload conditions without any characteristics variation.

Keywords: Diode-based Voltage-Limiter (DVL), Immittance Passive Resonant Tank (IPRT), Load Resonant Converter (LRC).

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1. INTRODUCTION

Load Resonant Converters (LRCs) [1], [2] are used widely as constant current or voltage sources in applications such as high-voltage power supplies [3], induction heaters [4], driver for illumination systems [5], electric arc welders [6], battery or capacitor chargers [7], [8], power factor correctors [9], and contactless power transfers [10]. Therefore, robust output against load variation is an important characteristic in the LRCs design [11], [12]. A simple and reliable technique to achieve load regulation ability in LRCs is utilization of Immittance Passive Resonant Tanks (IPRTs) in LRCs. This feature has been investigated deeply in previous works for IPRTs with various number of reactive component [13-16]. In this method, the robust load regulation capability can be achieved based on a topological technique; thus, utilization of complex controller can be eliminated. In the IPRT-based LRCs, the output voltage is varied according to the various load values and the output current remain constant based on the inherent load-independent operation of the IPRT in a defined switching frequency. An important problem in this type of the LRCs is occurs when the load increases. In this condition, the output voltage increases accordingly to control the output current in a predefined constant value. This phenomenon can damage the load or the LRC in a specific application such as chargers and electric arc welders. For example, in the battery charger that is charged with a constant current LRC, the output voltage should be limited to a defined voltage when the battery charging procedure is near to the full-load condition. Otherwise, the output voltage increases to high values and the battery lifetime is reduced. Or, in the electric arc welders, if the arc is offed, the open-circuit condition occurs and the LRC can be damaged due to very high output voltage [17]. Therefore, in the IPRT-based LRCs, a voltage clamper should be considered to protect the converter properly.

To solve the mentioned drawback, a method is applying a control circuit to tune the output voltage based on a predefined reference value. In this way, the complexity and cost of the LRC controller increases. An alternative technique is utilization of a clamping circuit, which limits the output voltage topologically. Based on this perspective, a simple circuit topology is presented in [17] using two clamping diode, which demonstrated in Fig. 1. As can be seen, if the IPRT output voltage is less than the V_{in}, two diodes are reverse biased; and if the IPRT output voltage is more that the V_{in}, two diode are direct biased and the output voltage is clamped to the V_{in}. Although, this circuit is not a general method for various IPRT topologies and conditions because a predefined assumption is considered, which the maximum output voltage of the IPRT in the full-load condition is equal to the V_{in}. This assumption is correct when the IPRT voltage gain is a specific value, which restricts degrees of freedom for the optimum design of the IPRT parameters value. Also, this topology is considered for clamping the output voltage to the V_{in}, while in some conditions it is wanted to clamp the output voltage to the higher values. In this paper, a new improve Diode-based Voltage-Limiter (DVL) is introduced, which have the follows feature that can be considered as its main features:

- It has high flexibility in variation the border of the clamping voltage that can be tunable according to the converter application and also can be applied in LRCs with various IPRT topologies.
- This flexible topological structure for voltage clamping has minimum number of components increment;
- The positive operation characteristics of the LRC, such as Zero Voltage Switching (ZVS) of the inverter switches and Zero Current Switching (ZCS) of the rectifier diode are preserved in case of utilizing DVL circuit.

Some other topologies have been offered in [17] with more operation flexibility. Although, they do not have the first circuit simplicity, reliability, and correctness, and also use the higher number of the components with more complicated structures. In [18] explores using a concept called duality to design new current-based DC-DC converters. Duality involves creating a mirror image of an existing circuit, where specific components are swapped. This paper applies this idea to traditional voltage-based DC-DC converters, including buck, boost, fly-back, cuk, sepic, and zeta designs. In [19] a tuneable band-pass filter built with an operational transconductance amplifier. This filter acts as an anti-aliasing filter for an analog-to-digital converter. An AAF is crucial to block unwanted signals before they reach the ADC, ensuring accurate digital conversion. Therefore, a new simple topology should be proposed to cover weaknesses of the presented circuit in Fig. 1 with the same simplicity.

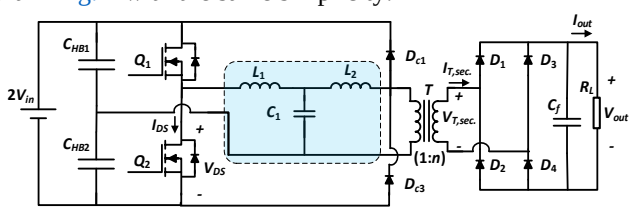


Fig. 1: The presented clamping circuit in [17]

2. PROPOSED DVL DESIGN

Table 1 provides samples of the appropriate type sizes and styles to use. The main paper sections must be organized as

follows: The new proposed DVL is presented in Fig. 2 to clamp the output voltage of a typical IPRT-based LRCs, named LCCLC-LRC. The fifth-order LCCLC-IPRT topology is a sample and can be replaced with the other IPRT structures. This DVL is composed of the two diodes, similar to Fig. 1, and only two extra zener diodes that connected two the previous diodes directly. Each pair of two diodes (a usual and a zener) are act in half cycle of the LRC operation. Therefore, by analyzing of a pair, the similar condition exists for the other pair.

In the positive cycle, if the IPRT output voltage is less than V_{in}, D_{c2} in Fig. 2 is reverse biased and LRC is operated in the usual condition. If the IPRT output voltage is more than V_{in}, D_{c2} is forward biased and the LRC will operated in the clamping mode based on the following expression:

$$V_{break,Dc1\&Dc3} = V_{pri,full} - V_{in} \qquad (1)$$

In which, $V_{pri,full}$ is the maximum output voltage of the IPRT in the full-load condition, and $V_{break,Dc1\&Dc2}$ is the breakdown voltage of the zener diodes that should be defined based on difference between the $V_{pri,full}i$ and V_{in} to limit the output voltage of the LRC to the full-load condition.

Expression (1) is true for the condition that DVL clamps the output voltage to the full-load condition. To obtain a higher value for clamping of the output voltage, the breakdown voltage of the zener diodes should be increased by a required extra voltage (V_{extra}), which is considered in problem description. In this condition, the breakdown voltage of the DVL zener diodes is defined as:

$$V_{break,Dc1\&Dc3} = (V_{pri,full} - V_{in}) + V_{extra} \qquad (2)$$

3. SIMULATION RESULTS

To demonstrate the proposed DVL ability and its operation correctness, a 150W LCCLC-LRC prototype with 300kHz switching frequency is considered as a sample circuit. In the designed converter, Vin=24V, Iout=3.5A, and RL=12Ω. The detail design procedure and analysis of the LCCLC-LRC have been introduced in [8] and to avoid from prolongation, the operation characteristics and components value are considered similar. Therefore, the value of the components, according to Fig. 2, are defined as: L1=L2=2.6μH, C1=C2=335nF, C3=168nF, Cf=47μF, and n (transformer turn ratio) =1.75. A 48V supply is applied due to using half-bridge inverter at the input of the converter.

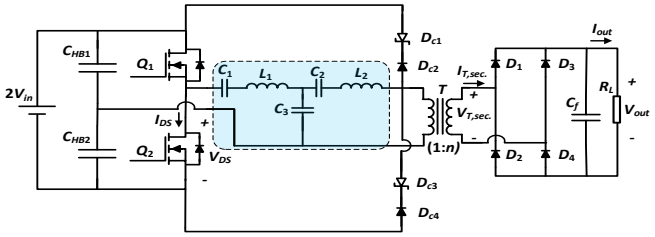


Fig. 2: The proposed DVL structure for output voltage clamping of the LCCLC-LRC

The OrCAD software is applied for simulation of the LCCLC-LRC due to high ability in real modelling of the components circuit with more accordance to real experimental conditions in comparison with the other simulator. The LCCLC-LRC schematic is presented in Fig. 3. IRFP150 is used as the inverter switches, and IR2113 is applied as the switches driver. A 1Ω resistor is used to model the ohmic losses of the LCCLC-LRC. LCCLC-LRC prototype is presented in Fig. 3. Operation waveforms of the designed LCCLC-LRC in nominal load are presented in Fig. 4. The LCCLC-LRC operation waveforms in half-load, full-load, and twice of the full-load conditions are presented in Fig. 5, for clamping the output voltage to the full-load case. Therefore, the breakdown voltage of the zener diodes is the difference between the maximum voltage of the IPRT output (43V) and Vin, which is equal to 18V according to (1). It is clear that the LCCLC-LRC has the normal operation in half-load and full-load conditions. In twice of full-load condition, the output voltage of the IPRT is clamped to 43V, which is the full-load condition voltage. Therefore, the LRC output voltage clamped to the predefined value in the full-load condition. As can be seen in Fig. 4, the voltage and current of the rectifier diodes are in phase and switching losses of this part is minimum. Also, the ZVS operation of the inverter switches is preserved in heavy loads. Thus, the switching losses in the inverter part is very low, and a low switching losses is due to the turn-off current of the switches.

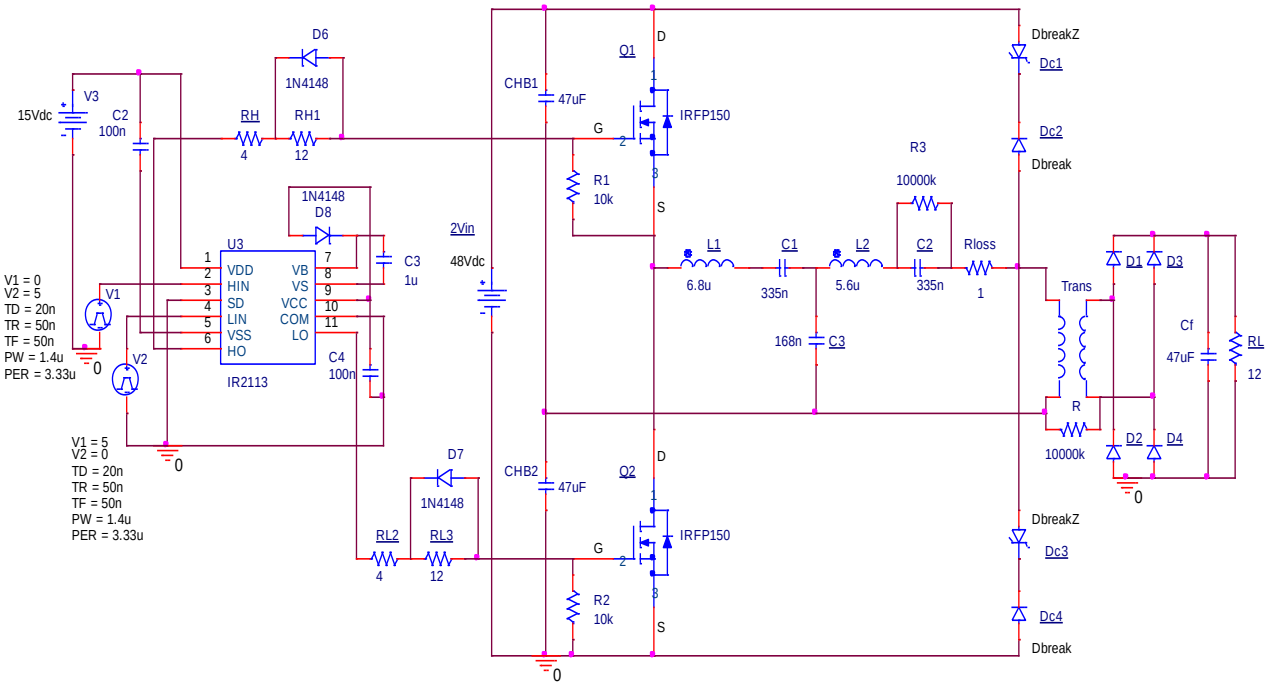
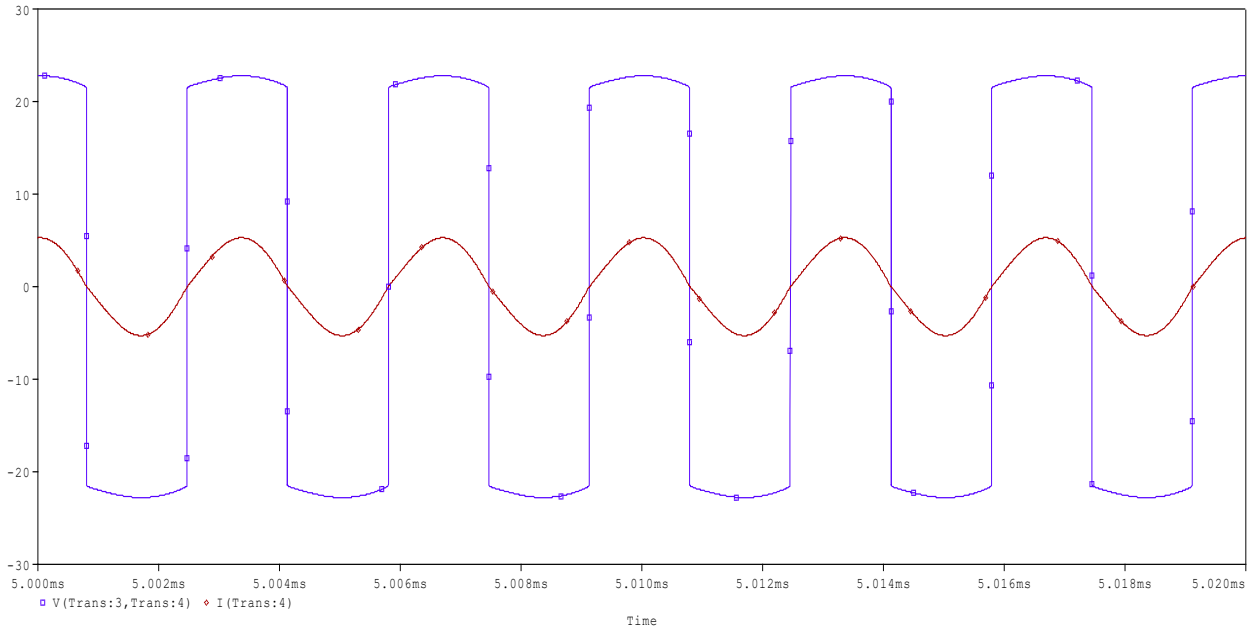
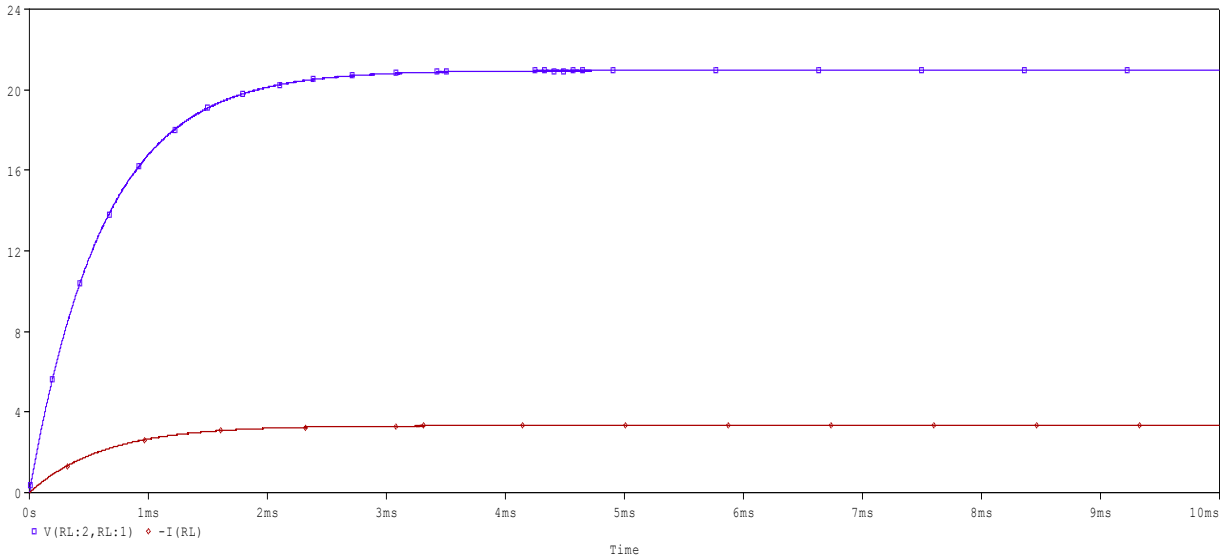


Fig. 3: The proposed DVL schematic circuit in OrCAD

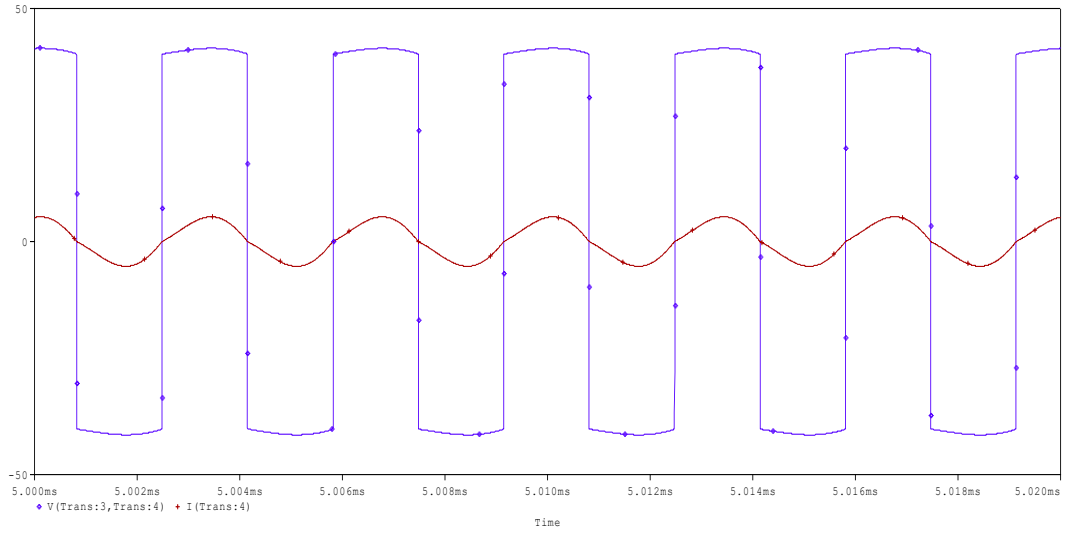


(a)



(b)

Fig. 4: Simulation waveforms of the LCCLC-LRC with the applied DVL in half-load condition for voltage claming in full-load. (a) Voltage and current at secondary side of the transformer; (b) output voltage and current. Blue: voltage, red: current.



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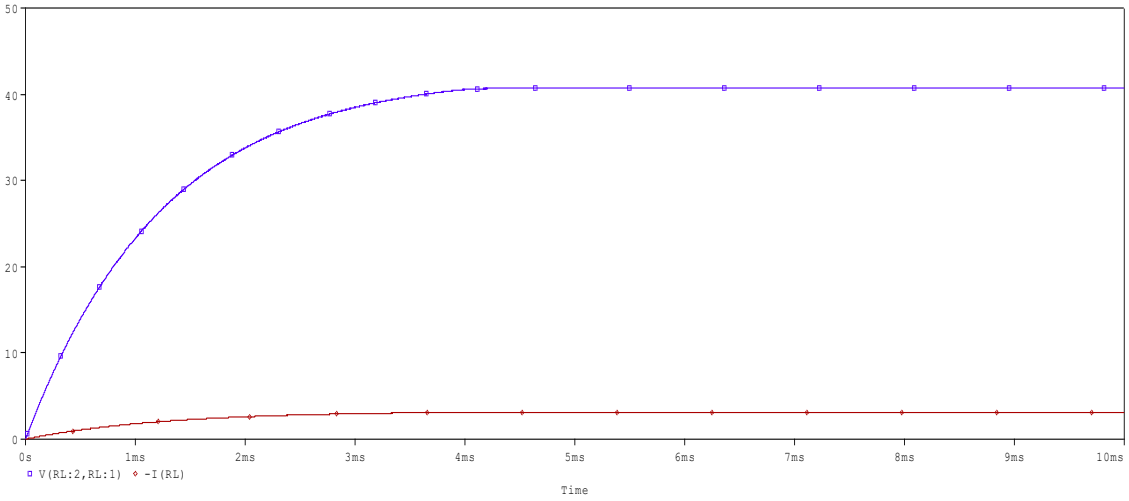
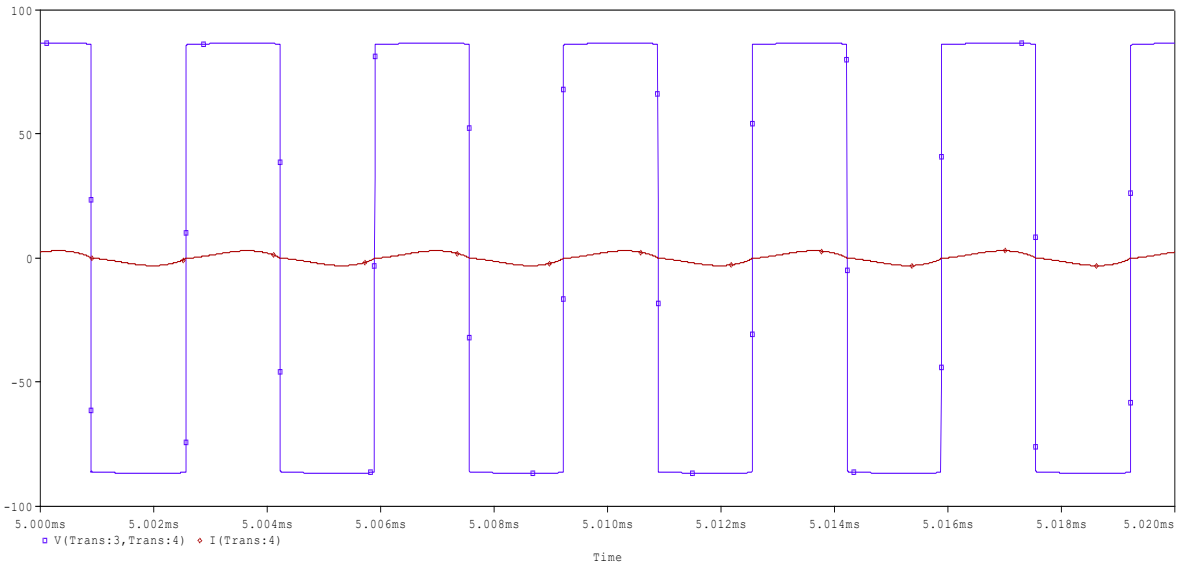
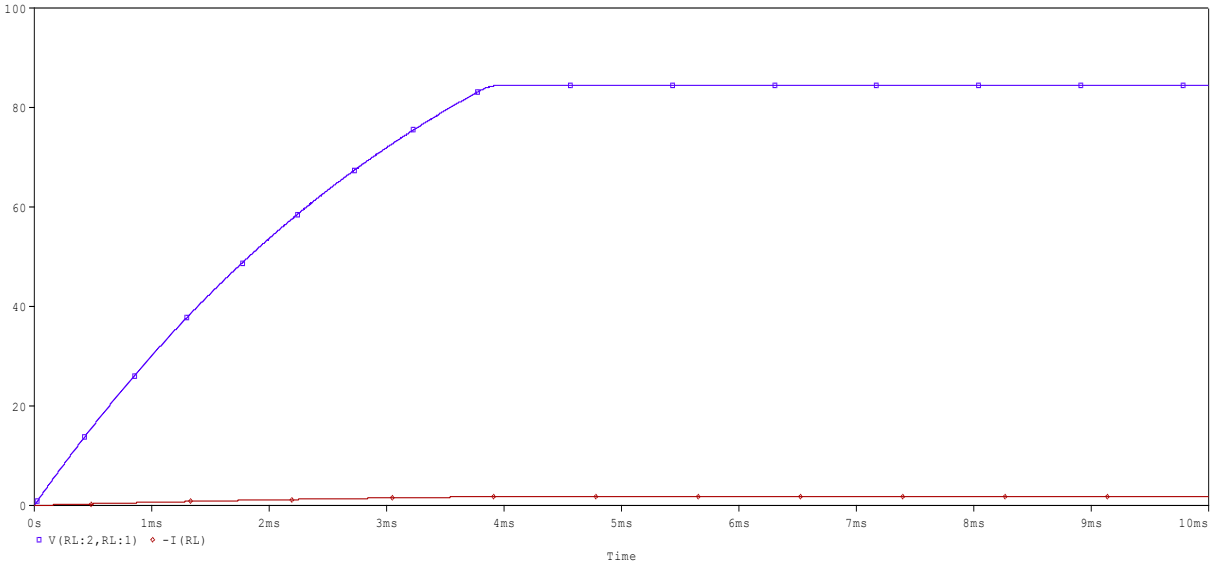


(b)

Fig. 5: Simulation waveforms of the LCCLC-LRC with the applied DVL in full-load condition for voltage clamping in full-load value. (a) Voltage and current at secondary side of the transformer; (b) output voltage and current. Blue: voltage, red: current.



(a)



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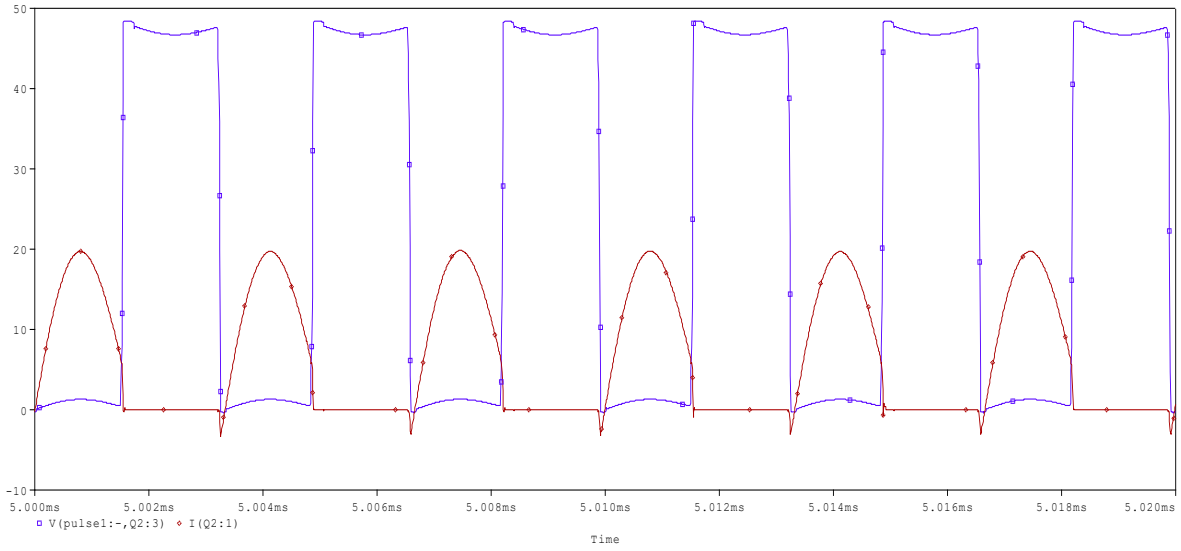

(c)

Fig. 6: Simulation waveforms of the LCCLC-LRC with the applied DVL in the three times full-load condition (36Ω) for voltage claming in twice the full-load value (86V). (a) Voltage and current in the secondary side of the transformer; (b) output voltage and current; (c) voltage and current of the inverter switch. Blue: voltage, red: current.

To demonstrate the flexibility of the proposed DVL for various limiting conditions, another simulation is performed for a higher voltage limitation than the full-load condition. In this case, the limitation value is considered in twice the full-load condition (86V). The simulation results are presented in Fig. 6. It can be seen that the output voltage is in the normal condition until R_L=24Ω. The output voltage is clamped to 86V in the higher values of the $2R_L$, such as 36Ω, without affecting the ZVS of the inverter switches and ZCS of the rectifier diodes. The output current and voltage of the LCCLC-LRC as a function of the R_L, are presented in Fig. 7 and also Fig. 8 respectively for voltage clamping in the full-load case. As can be seen, the output current is nearly constant in light- to full-load condition. When the load is higher than the full case, the constant current mode converts to the constant voltage mode. In this condition, the output voltage remain constant with the load increasing. Therefore, the output current decrease proportionally.

4. Conclusion

A new general diode-based circuit (DVL) is presented in this paper for clamping the output voltage of the constant current IPRT-based LRCs for protecting the load and converter in the heavy-load conditions. This topology is very simple and reliable with high precision. Due to applying only four diodes (two usual and two zener) the DVL cost and complexity is very low in comparison with other controller-based methods. The output voltage clamping ability of the proposed DVL is examined with a sample LRC (LCCLC-LRC) prototype that designed in the past works.

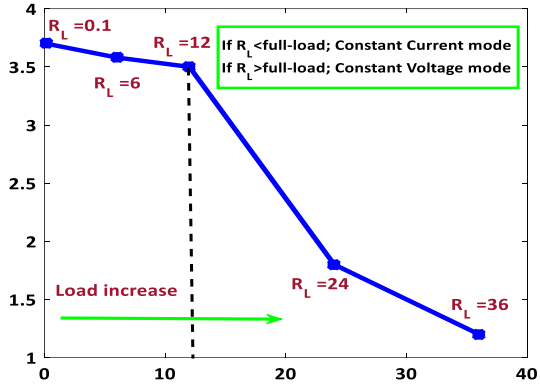

Fig. 7: LCCLC-LRC output current using DVL as a function of R_L.

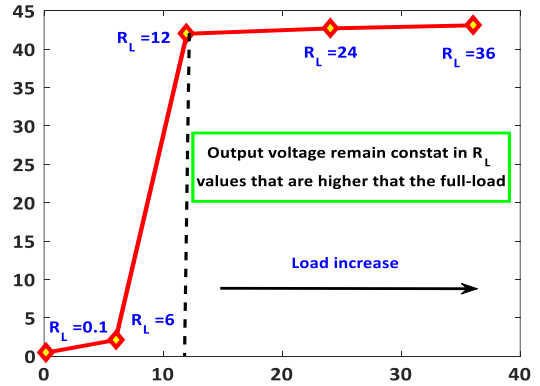

Fig. 8: LCCLC-LRC output voltage using DVL as a function of RL.

The simulation results, using the OrCAD and real model of the components, demonstrates that the introduced circuit can operate successfully in the various load values without affecting the main positive characteristics of the basic converter, such as ZVS of the inverter switches and ZCS of the rectifier diodes.

Credit Authorship Contribution Statement

Alireza Khoshsaadat: Conceptualization, Funding acquisition, Project administration. **Mohammad Abedini**: Data curation, Roles/Writing - original draft, Writing - review & editing.

Declaration Of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper. The ethical issues; including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, redundancy has been completely observed by the authors.

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BIOGRAPHY

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