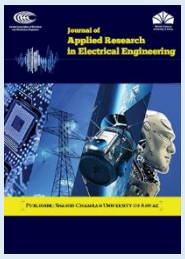
Shahid Chamran University of Ahvaz

Iranian Association of Electrical and Electronics Engineers

Journal of Applied Research in Electrical Engineering

E-ISSN: 2783-2864
P-ISSN: 2717-414X
Homepage: https://jaree.scu.ac.ir/



Research Article

Performance Analysis of a Steep-Slope Bi-channel GaSb-GaAs Extended Source Tunnel Field Effect Transistor With Enhanced Band to Band Tunneling Current

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Abstract: This paper presents a comprehensive investigation of the electrical properties of a heterojunction tunnel field effect transistor with enhanced electrical tunneling current. The proposed device structure incorporates an extended source region and two parallel channels positioned above and below the source region. This configuration effectively amplifies the tunneling area, leading to a significant improvement in the on-state current. Moreover, the inclusion of an embedded oxide region between the source and drain regions confers the device with a high resistance to short-channel effects. The combination of materials in both the source and channel region results in a staggered band alignment at the tunneling junction. This specific configuration leads to a lower threshold voltage for the initiation of tunneling. The impact of critical design parameters on the device performance has been thoroughly examined. A 2D variation matrix has been developed to compute the threshold voltage and on-state current variation based on the source doping density and gate workfunction, which serve as essential design parameters to optimize the electrical performance of the device. Furthermore, the device has achieved a unity current-ratio frequency of 300 GHz indicating its suitability for high-frequency applications. Additionally, the proposed structure provides an on-state current of 2.24×10^{-4} (A/μm), an off-state current of 1.24×10^{-15} (A/μm), an on/off current ratio of 1.81×10^{11}, and a subthreshold swing of 5 (mV/dec). These characteristics make the device viable for energy-efficient, high-speed digital circuits.

Keywords: Tunnel field effect transistor, band-to-band tunneling, workfunction, heterojunction.

Article history
Received 21 September 2023; Revised 08 January 2024; Accepted 28 January 2024; Published online 28 January 2024.

How to cite this article
Z. Ahangari, "Performance analysis of a steep-slope bi-channel GaSb-GaAs extended source tunnel field effect transistor with enhanced band to band tunnelling current," *J. Appl. Res. Electr. Eng.*, vol. 2, no. 2, pp. 206-213, 2023.
DOI: 10.22055/jaree.2024.44844.1082

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1. INTRODUCTION

The reduction in size of traditional Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) dimensions is the leading factor in the advancement of low-power high-speed integrated circuits. Nevertheless, when the MOSFET dimensions are scaled down to the nanoscale level, undesirable effects, commonly referred to as short channel effects, come into play, ultimately impairing device performance and elevating power consumption [1-6]. The conventional MOSFET is restricted by the thermionic electron emission-type transport and has a fundamental limit for the sub-threshold swing. However, Boltzmann limit dictates that it cannot be smaller than 60 (mV/dec) under room temperature conditions. In order to advance computational technology, a new class of devices is required. The Tunnel Field Effect Transistor (TFET), also known as the steep-slope device, is one of the most promising candidates.

It exploits interbond tunnelling, a quantum mechanical effect, as a transport mechanism. As a result, sub-thermionic transport can be achieved at room temperatures, along with low off current and a favourable on/off current ratio. The conventional TFET is a gated p-i-n diode that is reverse biased. The modulation of the tunneling barrier width at the interface of the source and channel region is achieved through the gate bias. When in the off-state, the tunneling barrier is sufficiently thick, and as a result, the carriers cannot tunnel through. However, by applying an adequate amount of bias to the gate, carriers of the opposite type with respect to the source region accumulate in the channel. This accumulation creates a steep p^+-n^+ tunneling junction with a thin barrier width that facilitates carrier band to band tunneling [7-10]. The initial TFET device suffers from low on-state current due to tunneling occurring only at a limited region at the interface of source and channel regions. However, recent studies have

shown that the band to band tunneling current of a TFET is dependent not only on the source doping density but also on the band gap of the material used in designing the device. Effective band alignment at the source-channel interface can amplify the tunneling rate. Homojunction TFETs employ similar materials at the tunneling junction, while heterojunction TFETs use different materials leading to different band alignments at the tunneling junction, including staggered gap and broken gap heterojunctions. A heterojunction formed by suitable semiconductor materials of different band gaps, mainly from group III-V, can be constructed and arranged to further boost the tunneling current [11-14]. Expanding the tunneling area is an additional approach, alongside material engineering, that can be employed to enhance the tunneling rate. Various structures such as L-shaped [15-17], F-shaped [18,19], and electron-hole bilayer TFET [20-22] and vertical TFET [23-25] exhibit an enlarged tunneling region. Nevertheless, the intricate nature of their fabrication process poses a challenge.

In this paper, a new heterojunction vertical tunnel field-effect transistor is presented with two parallel channels and an improved band-to-band tunneling region, leading to a significant enhancement in the on-state current of the device. The proposed device employs GaSb as the source material and high band gap GaAs in the channel and drain regions. Through the creation of a staggered heterostructure at the source/channel interface, a robust electric field is established, thereby facilitating band-to-band tunneling current with low transition voltage. In the proposed extended source TFET, band to band tunneling occurs across the thickness of the intrinsic channel and in the vertical direction, leading to a substantial increase in the tunneling area and a notable improvement in the on-state current. Furthermore, a comprehensive analysis is conducted to examine the influence of crucial design parameters on the device performance, and the corresponding electrical measures in the analog and digital domains are evaluated. Additionally, a 2D variation matrix of the threshold voltage and on-state current is generated to determine the ideal design parameters that promote optimal efficiency of the device. In prior investigations, the primary emphasis was placed on optimizing the electrical properties of a TFET device through the simultaneous attainment of the minimum possible off-state current, the lowest average subthreshold swing over a broad range of drain current, and the maximum achievable on-state tunneling current. In essence, in order to enhance the band-to-band tunneling current and establish a step-like transition from the off-state to the on-state, the transmission probability of the tunneling barrier must approach unity for a small deviation in the gate voltage around the threshold voltage. This necessitates a significant modulation of the energy bands through gate bias and an exceedingly thin tunneling barrier. Various approaches exist to enhance TFET performance, encompassing Doping Engineering [26-29], Material Engineering [30], as well as Geometry and Structure Engineering [31]. The TFET device in [23] examines the proposed vertical tunneling TFET based on silicon material. Essentially, owing to the relatively high effective mass of silicon, an alternative material combination becomes essential in order to amplify the tunneling rate. In [28], in contrast to the conventional TFETs with a p-i-n doping profile, both the source and channel regions possess a similar doping profile, which could potentially facilitate the fabrication process of the device. Nevertheless, the optimization of the gate workfunction and channel doping density is imperative in achieving efficient performance. In [30], a p-type electron-hole bilayer TFET with GaSb is introduced as a low-power device with an enhanced tunneling window. In [31], a three-dimensional nanowire TFET is proposed to enhance the gate controllability and boost the tunneling rate. Although the fabrication process for this device is complex, it leads to significant improvement in electrical characteristics. The device presented in this paper integrates the benefits of previously documented tunnel field-effect transistors (TFETs) to create a device with enhanced electrical efficacy. The device utilizes a heterojunction approach founded on material engineering principles, and a widened source region is utilized to amplify the rate of tunneling. The incorporation of a dual parallel channel introduces an additional tunneling junction that significantly enhances the on-state current.

The present paper is structured in the following manner: Firstly, the proposed TFET schematic along with critical simulation models are introduced in the subsequent section. Subsequently, the device performance outcomes and discussions regarding the crucial physical and structural design parameters are presented. Ultimately, the conclusion section provides an overview of the paper.

2. Device Structure and Simulation Set Up

The illustration of Bi-channel Extended Source Tunnel Field Effect Transistor (BESTFET) is depicted in Fig. 1. Fig. 1a displays the preliminary two-dimensional diagram of the BESTFET, while Fig. 1b portrays its on-state functionality by delineating the tunneling region in the parallel channel. The utilization of GaSb as a source material and high band gap GaAs in the channel and drain regions results in a lattice matched staggered type heterojunction that promotes band to band tunneling rate, as depicted. Experimentally, the utilization of the metalorganic vapor phase epitaxy (MOVPE) technique allows for the successful incorporation of carbon as a dopant in order to produce p-type GaSb. Moreover, the fabrication of p-GaSb can also be achieved through the diffusion process by introducing Zinc (Zn) as a dopant.

The aforementioned material combinations allow for the attainment of a high on-state current without any occurrence of ambipolarity in the suggested heterojunction device. The proposed BESTFET comprises two parallel channels with a significant band to band tunneling area. In contrast, conventional TFET experiences tunneling in a limited region near the gate oxide area at the source-channel interface, leading to inadequate on-state current. However, the BESTFET offers two parallel channels with an enhanced band to band tunneling area, which efficiently enhances the on-state current. The fundamental physical and structural design parameters of the structures investigated in this study are presented in Table 1. The Numerical simulations are conducted using the ATLAS device simulator [32], and the device performance is evaluated using the following models:

(1) Band to band tunneling; Basically, TFETs exploits the

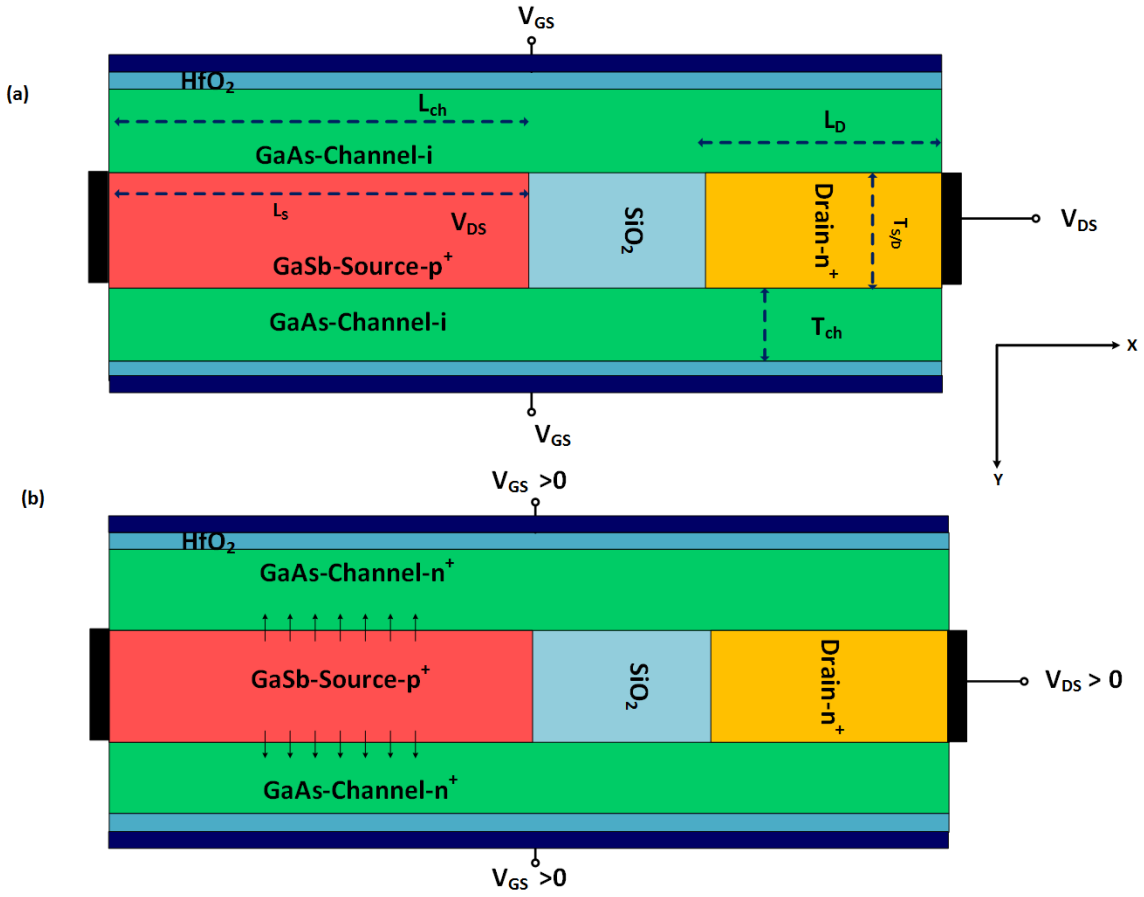

Fig. 1: (a) schematic of BESTFET with heterojunction material combination at the source and channel region, (b) on-state operation of BESTFET, in which tunneling occurs along the channel thickness in two parallel channels.

quantum mechanical phenomena better known as nonlocal band to band tunneling as the main current mechanism. In principle, band to band tunneling occurs when the channel conduction band aligns with the source valence band. Following the band alignment, energetic overlap emerge promptly which leads to a steep switching of the device from off-state to on-state. (2) Band gap narrowing; The energy band gap is a crucial factor that can significantly impact the rate of tunneling. Empirical evidence suggests that the contraction of the band gap takes place in regions with heavy doping because of the emergence of supplementary impurity bands caused by the overlapping of impurity states. (3) Mobility models; Mobility models take into account the effect of dopant density and lattice scattering on carrier mobility, as well as the influence of vertical and horizontal electric fields. In areas with high levels of doping, the mobility of carriers is reduced as dopant atoms serve as potent scatter centers, thereby diminishing the average time between collisions. Additionally, the carrier drift velocity and effective mobility can be significantly impacted by the electric field emanating from the gate and drain bias. (4) Trap assisted tunneling (or Shockley-Read-Hall recombination) models; It is evident that the process of band-to-band tunneling involves the movement of an electron from the valence band across the band gap to the conduction band. However, the occurrence of energy states within the band gap due to the presence of traps and defects can lead to tunneling before the onset of gate bias assisted band to band tunneling. Consequently, a decline in subthreshold swing can be expected. (5) The proposed BESTFET contains a channel region that is confined between the gate insulator and the source region according to the quantum confinement model. As the thickness of the channel scales down below 5nm, the quantum capacitance is affected by the finite number of density of states in the channel, leading to variations in the gate capacitance. Thus, appropriate quantum confinement models must be utilized to ensure accurate results.

Table 1: Initial physical and structural design parameters for the BESTFET.

Parameters	Value
Channel Length (L_{ch})	60nm
Extended Source Length(L_s)	30nm
Channel Thickness (T_{ch})	5nm
Gate Insulator Thickness-HfO_2	2nm
Source Doping Density	3×10^{19} (cm^{-3})
Channel Doping Density	intrinsic
Drain Doping Density	1×10^{18} (cm^{-3})
Gate Workfunction (WF_G)	4.0 eV
Source and Drain Thickness	5nm
Length of SiO_2	10nm

3. Results and Discussions

The energy band bending occurring at the interface between the source and channel regions can be roughly estimated as a barrier that resembles a triangle. Utilizing the Wentzel-Kramers-Brillouin approximation (WKB), the probability of tunneling in the BESTFET can be elucidated.

$$T_{WKB} \approx \exp(-\lambda \frac{4\sqrt{2m^*}E_G^{3/2}}{3q\hbar(E_G+\Delta\Phi)}) \quad (1)$$

where λ shows the tunneling length and shows the extension of the transition region at the interface of source and channel regions, E_G denotes the bandgap energy of the source region and $\Delta\Phi$ represents the tunneling window, where the BTBT is allowed to occur and m^* is the carrier effective mass. Essentially, the smaller value of λ demonstrates a more pronounced band bending at the tunneling region. From a theoretical standpoint, the increase in gate bias regulates the tunneling probability, T_{WKB}, through the reduction of λ and simultaneous increment of the $\Delta\Phi$ window. To enhance the operational effectiveness of TFET, it is imperative to meticulously engineer the tunneling junction in order to ensure a high BTBT rate and exceptional gate controllability across the tunneling barrier. In simpler terms, the tunneling barrier should be sufficiently thin to initiate tunneling. The energy band diagram for the BESTFET is presented in Fig. 2 for both the off-state (V_{GS}=0V V_{DS}=1V) and on-state (V_{GS}=1V V_{DS}=1V) conditions from the source to the channel. In the off-state, the electron density within the channel is inadequate to generate a narrow tunneling barrier, resulting in an absence of tunneling. However, when the gate voltage surpasses the threshold voltage value, the energy band within the channel is pulled down, and a significant reduction in the tunneling barrier at the source-channel interface is observed. Based on the energy band diagrams, the tunneling barrier width in the off-state is approximately 5nm, ad by employing the gate bias in the on-state, this barrier reduces to 3nm. Due to this phenomenon, there is a significant surge in the drain current which happens suddenly, resulting in a subthreshold swing that is much lower compared to the conventional MOSFET Boltzmann limit. Threshold voltage, as defined, is the minimum gate voltage necessary to initiate tunneling, leading to a rapid increase in drain current from the off-state to the on-state. Fig. 3 illustrates the density of both electrons and holes in the BESTFET device, both in the off-state and on-state. Essentially, in the absence of the gate bias, the electron density in the channel is insufficient for the creation of a sharp tunneling junction. Nonetheless, through the application of a positive bias to the sidewall gates, a build-up of electrons within the channel enables the formation of a thin tunneling barrier to facilitate tunneling. Fig. 4 displays the impact of drain bias variation on the transfer characteristics of the BESTFET. It is observed that the threshold voltage and off-state current of the device remain unaffected by drain bias variation. Tunneling field-effect transistors suffer from a major issue of drain induced source tunneling (DIST), wherein the electric field lines arising from the drain electrode affect the tunneling barrier width at the source and channel region interface in the absence of gate bias. However, the proposed structure deals with this issue by separating the drain region from the tunneling junction using a thick oxide layer, which significantly reduces the DIST effect. It is evident that the carrier velocity and, correspondingly, the on-state current increase as the drain bias is incremented. The subthreshold swing (SS) in the proposed device can be approximately defined as:

$$SS \approx \frac{\ln(10)}{q} W \quad (2)$$

in which q is the basic electric charge, W is defined as the tunneling barrier width. Essentially, as the gate bias is elevated towards adequately positive magnitudes, the width of the tunneling barrier is fundamentally diminished. This signifies the emergence of tunneling and a substantial reduction in the subthreshold swing. The subthreshold swing is precisely defined as the gate bias needed to achieve a six-fold change in the drain current, spanning from the minimum off-state current. The results demonstrate that for V_{DS}=1V, 2.24×10^{-4} (A/μm), an off-state current of 1.24×10^{-15} (A/μm), an on/off current ratio of 1.81×10^{11}, and a subthreshold swing of 5 (mV/dec) can be achieved, which makes this device feasible for high-speed low-power digital applications.

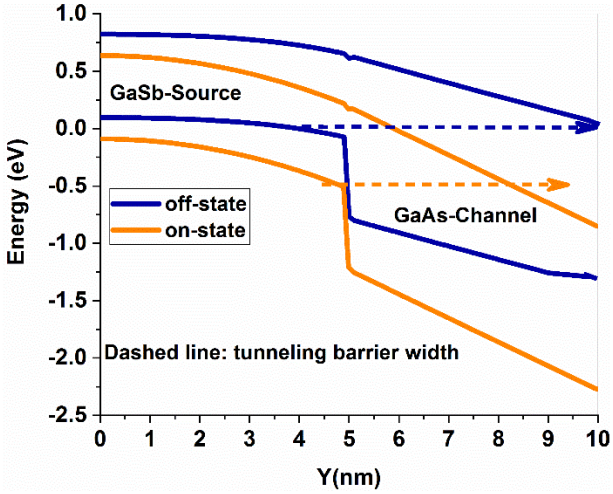

Fig. 2: Energy band diagram of the BESTFET in the off-state and on-state operation along the vertical direction from the source region towards lower channel region.

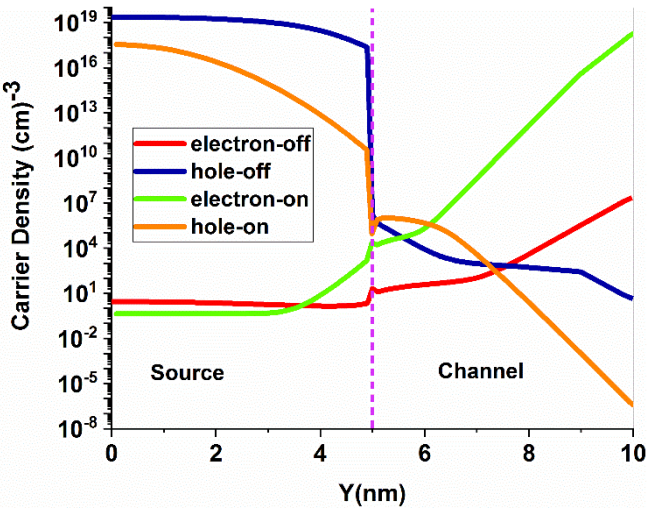

Fig. 3: Carrier density along the vertical direction from the source to lower channel region in the off-state and on-state.

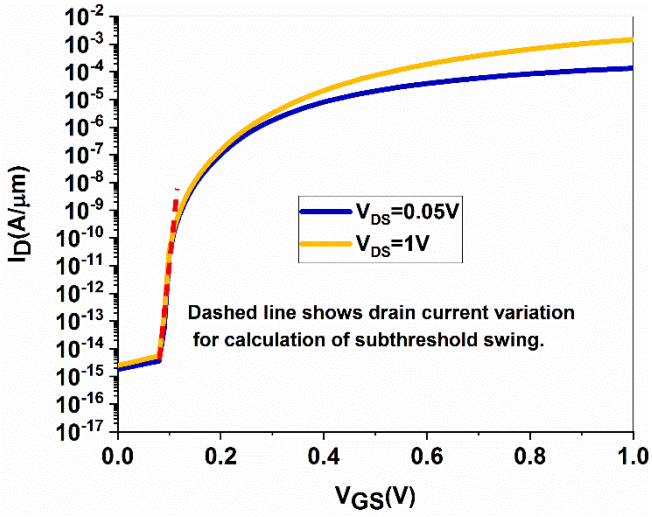

Fig. 4: Transfer characteristics of BESTFET as the drain bias is varied.

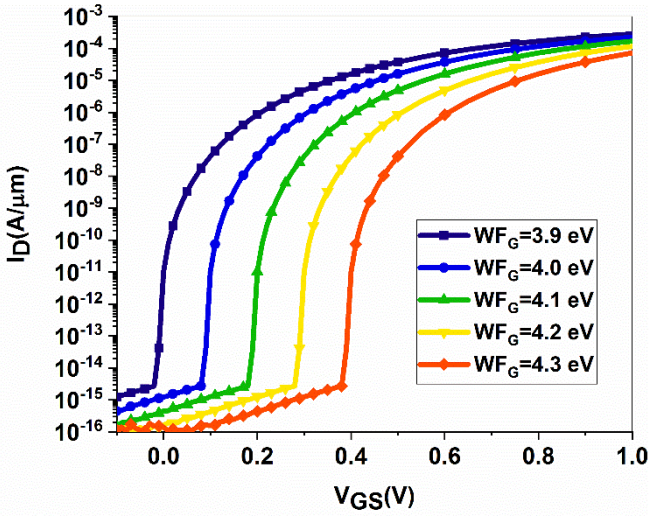

Fig. 5: Transfer characteristics of BESTFET as the gate workfunction is parametrized, V_{DS}=1V.

Fig. 5 depicts the transfer characteristics of the BESTFET with respect to the parametrization of the metal gate workfunction. Following materials are considered for the gate electrode: Hafnium (3.9eV), Zirconium (approximately 4eV), Indium (4.1 eV), Molybdenum (4.2 eV) and Titanium, Silver, Niobate (4.3 eV). It is evident that the distinction between the workfunction of the gate and the channel can indeed influence the carrier density within the channel. The findings indicate that an increase in the gate workfunction results in a reduced electron density in the channel, leading to a shift in the on-state to off-state transition voltage towards higher positive values. It is imperative to note that a narrow tunneling barrier necessitates a sufficient electron density. As such, a gate workfunction engineering framework is necessary for optimal device performance with a minimal threshold voltage value.

In order to initiate tunneling, a sharp p^+-n^+ tunneling junction is fundamental. The density of doping in the source is a crucial factor that can impact the tunneling rate. The transfer characteristics of BESTFET are depicted in Fig. 6, which demonstrates the effect of source doping density. The findings reveal that decreasing the source doping density leads to a significant increase in the threshold voltage and a decrease in the tunneling rate. The thickness of the space charge region at the interface of the source and channel regions is inversely related to the doping concentration of the source region. It is clear that a high concentration of dopants in the source region reduces the width of the tunneling barrier, thus increasing the electric field at the primitive gate electric field. Consequently, the increased electric field across the tunneling junction results in an elevation of the tunneling current. Therefore, to achieve a sharp tunneling junction and minimize resistance in the source region, a higher doping density should be utilized. The proposed device is characterized by an extended tunneling window that is situated at the interface of the source and channel region. The on-state and off-state variation with respect to the length of the extended source region is illustrated in Fig. 7. It is observed that the on-state current increases considerably as the Ls increases, which is indicative of an increment in the

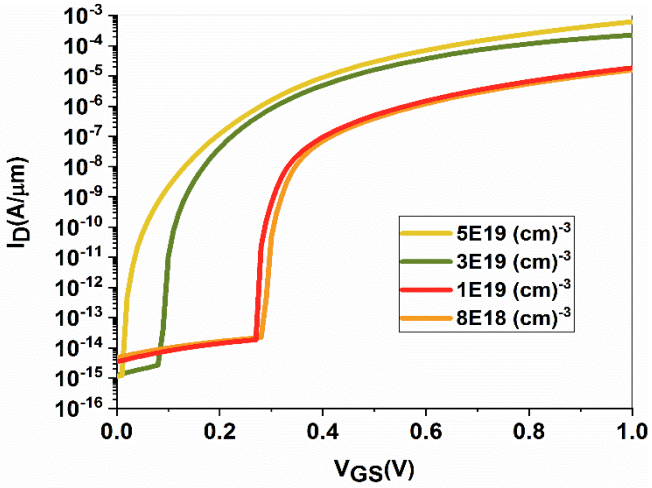

Fig. 6: I_D-V_{GS} curves of BESTFET as the source doping density is varied, V_{DS}=1V.

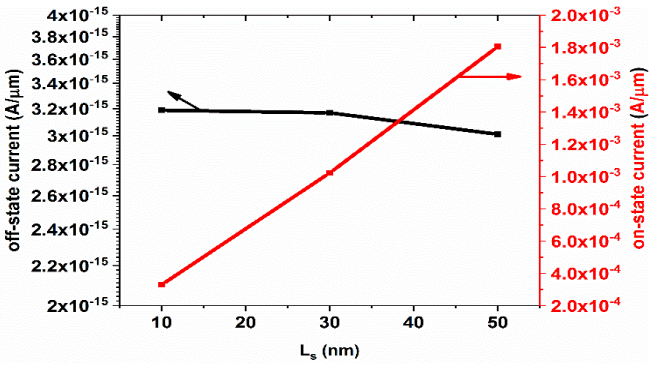

Fig. 7: Off-state and on-state current variation of the BESTFET versus source length.

band to band tunneling rate. Conversely, the off-state current exhibits negligible variation with respect to L_s. This is due to the embedded oxide region that lies between the channel and the drain side, as well as the wide band gap of the drain region, which limit the effect of the drain electric field on the tunneling rate.

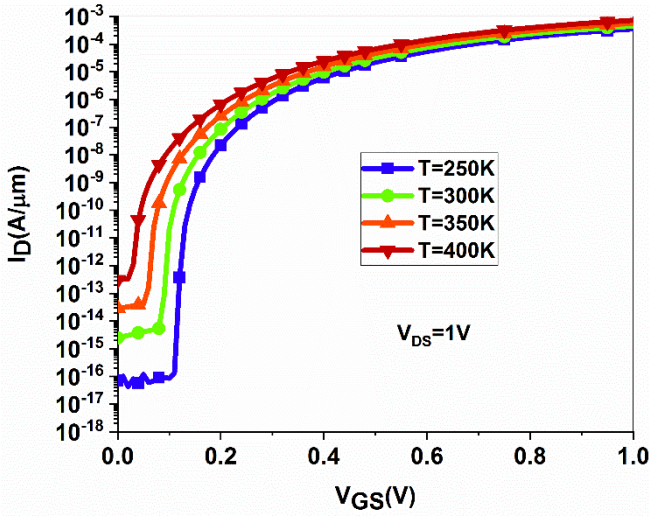

Fig. 8: Transfer characteristics of the BESTFET as the temperature is parametrized, V_{DS}=1V.

Temperature, a fundamental physical measure, has a profound impact on device performance as illustrated in Fig. 8 that showcases the effect of temperature on the transfer characteristics of BESTFET. It is evident that temperature has a notable influence on the off-state current and threshold voltage, while the on-state current shows a negligible variation. Specifically, an increase in temperature causes a variation in the density of minority carriers in the source region, leading to a contribution of minority electrons to the leakage current. In addition, scattering resulting from imperfections in the crystal structure, such as ionized impurities, assumes as the dominant mechanism when temperatures are low. Due to the decreased agitation of the atoms in the cooler lattice, scattering within the lattice becomes less significant. However, the motion of the carriers also slows down. Considering that a carrier moving at a slower pace is more likely to experience a stronger scattering effect when interacting with a charged ion compared to a carrier with higher momentum, events of impurity scattering lead to a reduction in mobility as the temperature decreases. However, in the on-state, the tunneling current predominantly consists of majority carriers and hence temperature does not have a significant effect on the drain current.

The findings indicate that the gate workfunction and source doping are crucial design parameters that significantly impact the p^+-n^+ tunneling junction, leading to a modification in the tunneling rate. In Fig. 9, the 2D variation matrix of the threshold voltage and on-state current is computed as a function of source doping density and gate workfunction. The point of maximum threshold voltage is situated in the uppermost left-hand corner of the variation matrix, indicating that a combination of a high gate workfunction value and low source density leads to an increase in the width of the depletion layer at the tunneling junction. To attain the lowest possible positive threshold voltage and high on-state current with steep subthreshold swing for n-type TFET, a sharp p^+-n^+ tunneling junction is essentially required. The variation matrix reveals that the proper combination of source doping density and gate workfunction in the bottom right side of the contour can be adjusted to achieve the lowest possible positive threshold voltage. Consequently, decreasing the transition bias for the onset of tunneling can result in maximum drain current, which can be observed in the bottom right corner of the variation matrix. It is noteworthy to state that the implementation of a heavily doped region in the source region can serve as a means to decrease the parasitic resistance of the source. Additionally, the manipulation of the gate workfunction engineering framework can be utilized to adjust the threshold voltage and thus the on-state current.

The illustration of the frequency response of the apparatus is evident in Fig. 10. The results demonstrate the achievement of a unity current-ratio frequency of 300GHz, thereby emphasizing the feasibility of employing the device in high-frequency applications. The proposed device possesses two sidewall channels as well as an extended source region. The presence of a thin film channel region leads to the existence of capacitance between the gate and the source/drain electrode. This capacitance plays a crucial role in the degradation of the current gain at high frequency. At high frequency, the impedance of the gate and the source/drain capacitance deteriorates, resulting in a decline in the current gain. This decline occurs due to the inability of the gate bias to effectively modulate the width of the tunneling barrier.

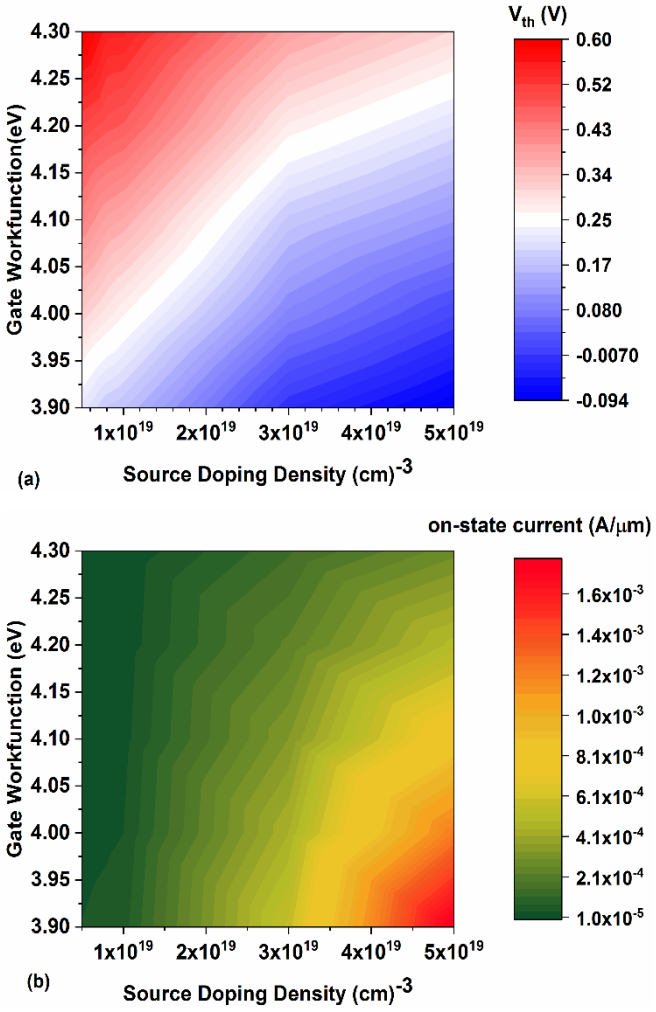

Fig. 9: (a) 2D variation contour of threshold voltage, (b) on-state current variation as a function of source doping density and gate workfunction value.

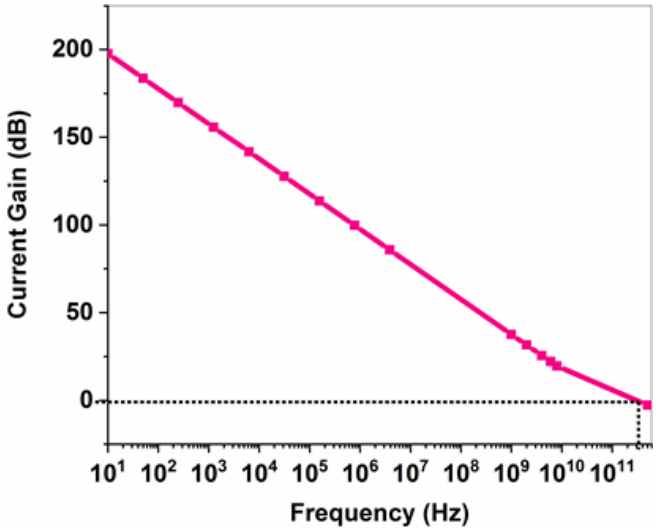

Fig. 10: Current gain versus frequency of the BESTFET for calculating the unity current-ratio frequency of the device.

4. Conclusion

In this study, a bi-channel TFET device with two sidewall parallel channels is subjected to a comprehensive analysis of its electrical characteristics. The study also evaluates the influence of crucial structural and design parameters on the device's performance. The findings showcase the device remarkable resistance to short channel effects, thereby highlighting its suitability for employment in the nanoscale regime. Furthermore, the gate workfunction and source doping density emerge as critical design parameters that significantly impact the device's performance. A 2D variation contour is computed for the threshold voltage and on-state current, taking into account the gate workfunction and source doping density variation. The results reveal that in order to attain a low-power high-speed TFET device, the source region should possess a high doping density. Additionally, the electrical performance of the device can be optimized through precise gate workfunction engineering framework.

CRediT Authorship Contribution Statement

Zahra Ahangari: Conceptualization, Data curation, Formal analysis, Funding acquisition, Investigation, Methodology, Project administration, Resources, Software, Supervision, Validation, Visualization, Roles/Writing - original draft, Writing - review & editing.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper. The ethical issues; including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, redundancy has been completely observed by the authors.

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