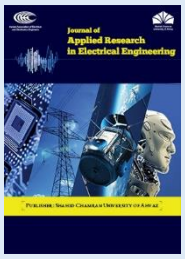
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Research Article

Design of a Tunable 4th Order OTA-C Band-Pass Filter for use in Front-End of ADC

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Abstract: This article presents a tunable fourth-order band-pass filter that is designed using operational trans-conductance amplifier (OTA), which can be used as an anti-aliasing filter (AAF) in the front-end of an analog to digital converter (ADC). It is necessary to use a suitable filter to prevent unwanted signals from entering the ADC. The bandwidth of the AAF should be designed according to the bandwidth of the ADC, therefore, matching these two bandwidths is one of the important challenges when using multi-bandwidth analog to digital converters in the digital communication applications. The proposed band-pass filter is designed and simulated in 180nm CMOS technology. The simulation results show that by changing the two bias voltages of the proposed filter, its bandwidth can be changed according to the frequency range of ADSL, ADSL2 and ADSL2+ communication standards and it effectively attenuates unwanted signals.

Keywords: Anti-aliasing filter, multi-bandwidth ADC, OTA-C filter, ADSL technology.

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1. Introduction

In order to use the continuous values in digital systems, analog to digital converters should be used. Analog to digital converters are circuits that convert continuous analog signals into discrete digital data [1, 2]. Digital cameras, biomedical applications and communication devices such as mobile phones and ADSL (Asymmetric Digital Subscriber Line) modems are devices that use an ADC [3-6]. Analog to digital converters have a structure similar to the block diagram in Fig. 1. In order to convert an analog signal to digital codes, first the input signal is passed through an anti-aliasing filter to prevent unwanted signals from entering the converter. Then, the output of this filter is sampled by the sampler circuit (for example: a sample and hold circuit) and sent to the next part, the quantizer, and according to the voltage level of each sample, a corresponding digital code is produced [2].

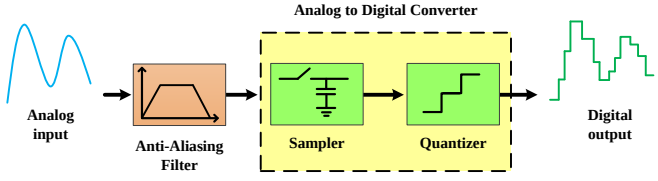


Fig. 1: Analog to digital converter block diagram.

Most ADCs need anti-aliasing filters, because according to the intended application, these filters can weaken some unwanted signals that are not in the required bandwidth of the converter. The passage of these signals reduces the performance of ADC [7]. On the other hand, new tunable ADCs that have the ability to change the bandwidth of their operation have been presented [8], which are used in various applications. In some digital communication systems, analog to digital converters should be able to change their bandwidth according to the need, in which a tunable anti-aliasing filter will be required. For example, ADCs used in communication devices that use ADSL technique must have the ability to convert in the bandwidths required by ADSL, ADSL2 and ADSL2+ standards, so it is necessary at the input of these types of converters and a proper tunable anti-aliasing filter should be placed in the front-end of the ADC [9, 10]. This paper is structured as follows: Section 2 describes the proposed band-pass filter architecture and its circuit details. Section 3 presents the simulation results, and finally Section 4 ends this paper with the conclusion.

2. Structure of the Proposed Band-Pass Filter

The block diagram of the proposed tunable fourth-order

band-pass filter is shown in Fig. 2. As shown in this figure, the structure of this filter consists of a low-pass and a high-pass filters, which their cut-off frequency can be adjusted by the external bias voltages of V_{b1} and V_{b2}.

2.1. Circuit Analysis of the Proposed Tunable OTA-C Filters

The OTAs which are actually known as differential voltage controlled current source (DVCCS). The value of "g" that shows their transconductance is calculated as follows (1):

$$g = \frac{I_{out}}{V_{in}} \quad (1)$$

Where I_{out} represents the output current and V_{in} is the value of the input voltage. The value of "g" can be mentioned as an essential parameter in the design such as active resistive capacitor (RC) circuits in which R is an important design parameter, and it is usually represented by an adjustable bias current (I_{bias}). The electronic adjustability of a circuit is one of the critical points that must be taken into account in a design to meet various design specifications [11, 12]. Due to the ability to adjust the transconductance in OTA, this type of amplifiers and capacitors are used in the OTA-C filter design. The OTA-C filters are categorized into two general structures, single output [13] or multiple outputs [14] with different types of designs. This research focuses on single output OTA-C filters. The proposed band-pass filter consists of two OTA-C fourth order low-pass and high-pass filters. To simplify the description of the operation of these filters, their second-order circuits are shown in Fig. 3.

The transfer function of these filters show the dependency of their cut-off frequency to the trans-conductance of OTAs. The transfer functions of the second-order high-pass and low-pass filters are shown in equations (2) and (3), respectively:

$$TF = \frac{S^2 C_1 C_2}{S^2 C_1 C_2 + S C_1 g_{m1} + g_{m1} g_{m2}} \quad (2)$$

$$TF = \frac{g_{m1} g_{m2}}{S^2 C_1 C_2 + S C_1 g_{m1} + g_{m1} g_{m2}} \quad (3)$$

Where g_{m1} and g_{m2} are the trans-conductance of the first and second amplifiers and C_1 and C_2 are the capacitors used in the proposed circuits. Assuming that the trans-conductance of OTAs and the capacitance of capacitors are equal, the cut-off frequency of the high-pass and low-pass filters (ω_0) is obtained from equation (4):

$$\omega_0 = \frac{g_m}{\sqrt{c_1 c_2}} \quad (4)$$

According to equation (4), the trans-conductance of OTAs can be changed by altering the bias voltage, thus the cut-off frequency of the filters can be tuned using the bias voltages.

The frequency response of the second-order high-pass and low-pass filters are shown in Figs. 4 and 5, respectively. As shown, by changing the bias voltage in the range of 0.3 - 0.8 volts, the cut-off frequency in the high-pass filter is adjusted between 10 kHz - 5 MHz, and in the low-pass filter, by adjusting the voltage between 0.3 - 0.8 volts, the cut-off frequency is changed between 12 kHz - 4 MHz.

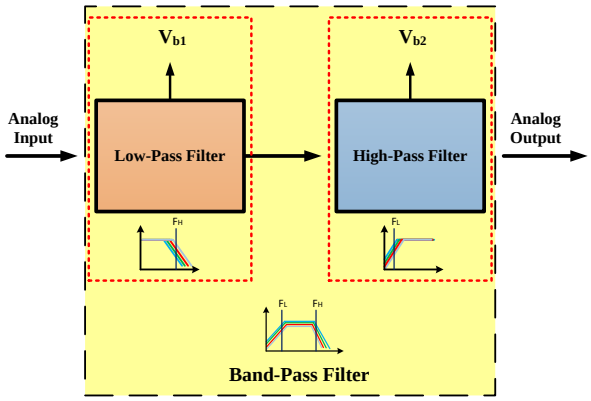


Fig. 2: Block diagram of the proposed band-pass filter.

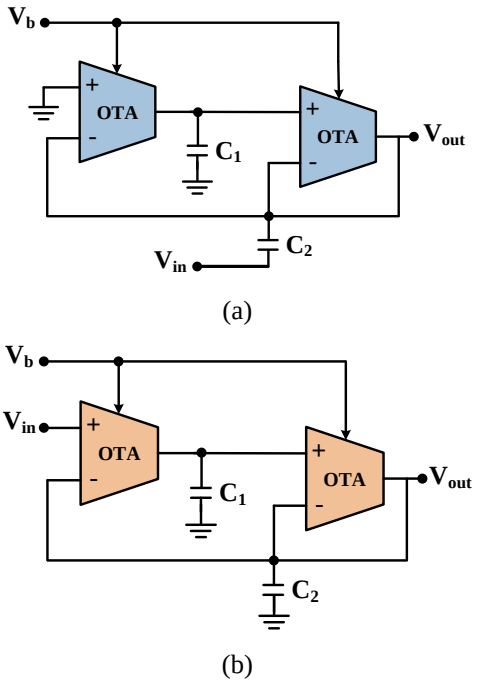


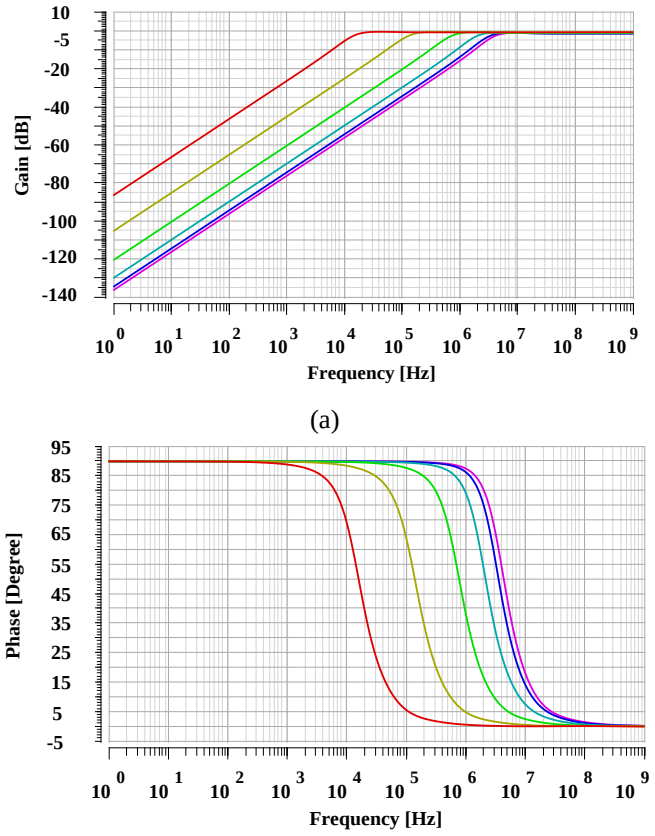
Fig. 3: Circuit schematic (a) high-pass (b) low-pass filter used in the proposed band-pass filter.

2.2. Proposed Transconductance Amplifier Circuit

The proposed transconductance amplifier that is used in the high-pass and low-pass filters is shown in Fig. 6. In the proposed amplifier, the trans-conductance value can be adjusted with changing of the bias voltage (V_b). The proposed differential transconductance amplifier has an output gain of 91 dB, a bandwidth of 6.8 MHz, and a phase margin of 75 degrees, and a common-mode rejection ratio (CMRR) of 105 dB. Fig. 7 shows the gain and phase diagram of the transconductance amplifier. Table 1 shows information such as the sizing of the OTA-C used transistors, the drain currents and the calculated trans-conductance values for each transistors.

2.3. The Structure of the Proposed Band-Pass Filter

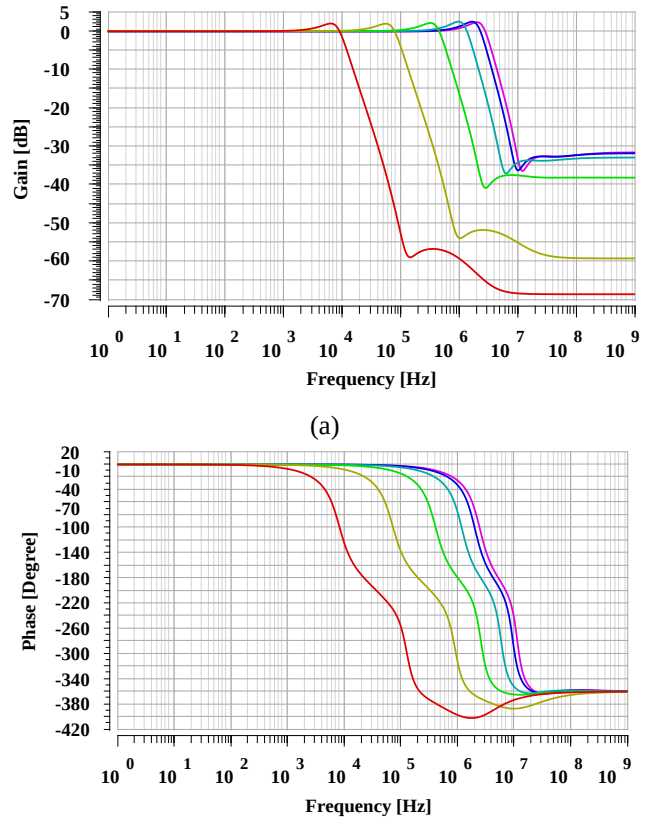
The OTA-C fourth-order band-pass filter circuit with adjustable feature using two high-pass and low-pass filters is



(a)

(b)

Fig. 4: Frequency response of the desired second-order high-pass filter including (a) gain and (b) phase.



(a)

(b)

Fig. 5: Frequency response of the desired second-order low-pass filter including (a) gain and (b) phase.

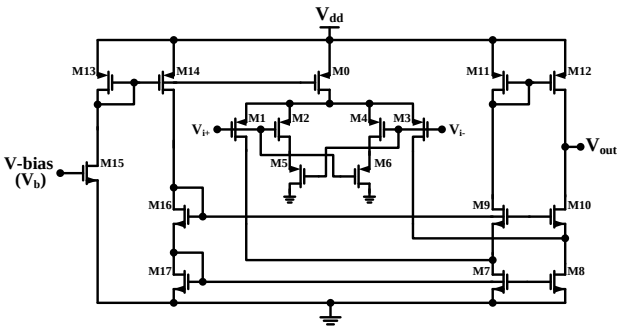
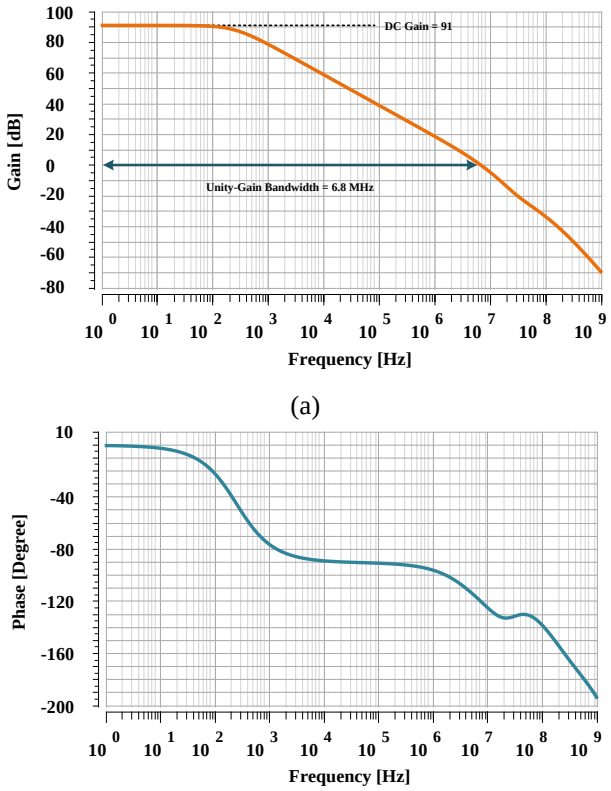


Fig. 6: Proposed trans-conductance amplifier circuit.



(a)

(b)

Fig. 7: The frequency response of the proposed operational trans-conductance amplifier for V_b = 0.6V including (a) gain and (b) phase.

Table 1: The parameters of transistors in the proposed OTA

Transistor	W(μm)	L(μm)	M	$I_d(\mu A)$	$V_{d_{Sat}}(mv)$	$g_m(\mu S)$
M_0	4	2	7	6.15	210	83.5
M_1 M_3	2	2	6	1	106	31.5
M_2 M_4	2	2	6	2.1	106	11.1
M_5 M_6	2	2	6	2.1	81.2	18
M_7 M_8	2.5	2	3	4.74	106.5	77.5
M_9	2.5	2	1	2.7	132.3	37.8
M_{10}	2.5	2	1	2.7	131.4	38.2
M_{11} M_{12}	4	2	7	2.7	86.5	45.7
M_{13} M_{14}	4	2	7	6.2	119.3	84.5
M_{15}	2.25	2	2	6.2	141.7	83
M_{16} M_{17}	2	2	5	6.2	108	102

presented in Fig. 8. By changing the bias voltages of the trans-conductance amplifiers, the cut-off frequencies of the filter can be tuned. Table 2 shows the relation between the filter cut-off frequencies and the bias voltages. In the proposed band-pass filter circuit, the capacitance of the used capacitors is 5 pF.

3. Simulation Results

The proposed band-pass filter was designed and simulated with CMOS 180nm technology at the transistor level. The proposed filter is tunable and its cut-off frequencies can be changed by adjusting the gm values of the OTAs using the bias voltages. There are two bias voltage settings of the proposed filter for working frequencies of special telecommunication standards, ADSL1 and ADSL2, are presented in Table 2. Also, the frequency responses and multiple simulation results of the proposed adjustable band-pass filter by setting the bias voltages are shown in Table 2 and Fig. 9, respectively. As shown in Fig. 9, the bandwidth of the proposed filter will be tuned with changing of the bias voltages. The layout of the proposed band-pass filter is shown in Fig. 10. The dimensions of the design are 573 um by 575 um, the area occupied by the proposed circuit is equal to 0.32 mm^2. Also, with specified bias voltages, the frequency responses related to the post-layout simulation of the proposed filter are shown in Fig. 11. By comparing the output results obtained from the post-layout and the pre-layout simulations of the proposed filter, it can be concluded that the frequency responses of the two are almost the same except for the attenuation in the upper stop band. The results of post-layout simulation are shown in Table 3.

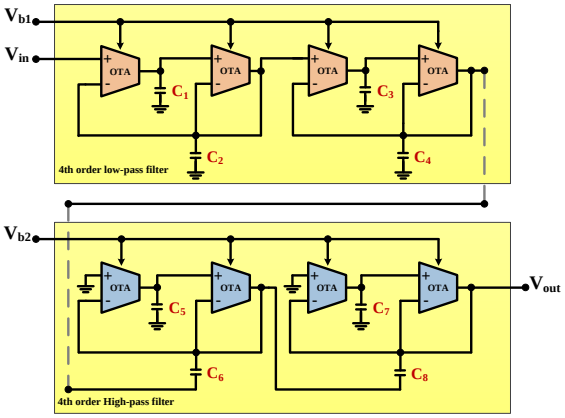


Fig. 8: Proposed fourth-order band-pass filter circuit.

Table 2: Frequency values required by changing the bias voltage for different applications in Pre-Layout simulation.

Curve	V_{BIAS1} (V)	V_{BIAS2} (V)	Low cut-off frequency (kHz)	High cut-off frequency (MHz)
ADSL 1	0.5	0.5	32	1.1
ADSL 2	0.5	0.6	32	2.2
Custom	0.28	0.52	11	1.3

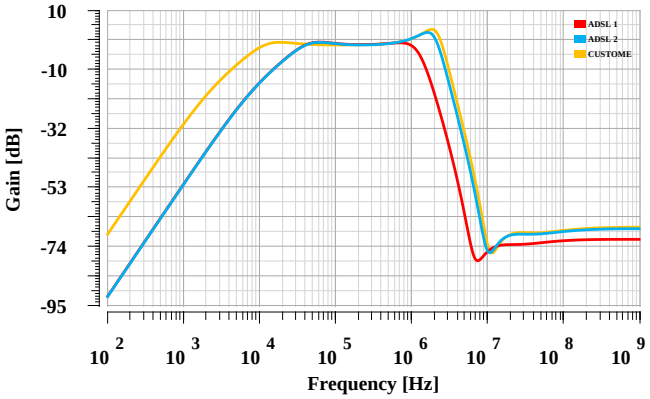


Fig. 9: The frequency response of the proposed filter for the bias voltage presented in Table 2.

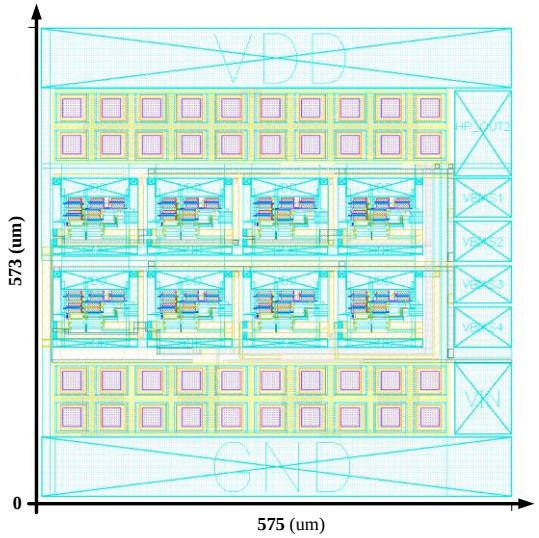


Fig. 10: Layout of the proposed band-pass filter.

Table 3: Frequency values required by changing the bias voltage for different applications in Post-Layout Simulation.

Curve	V_{BIAS1} (V)	V_{BIAS2} (V)	Low cut-off frequency (kHz)	High cut-off frequency (MHz)
ADSL 1	0.5	0.5	35	1.04
ADSL 2	0.5	0.6	33.2	2.15
Custom	0.28	0.52	18	1.19

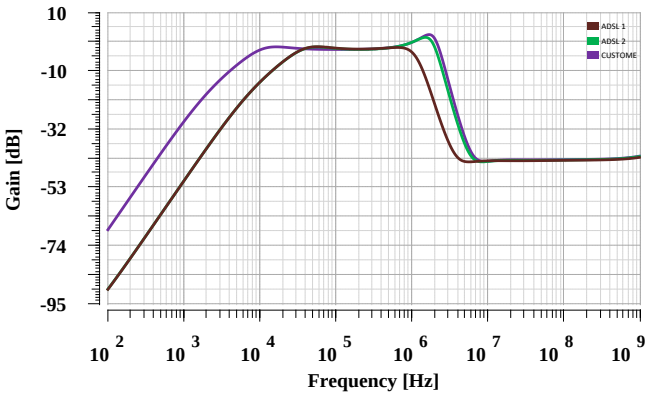
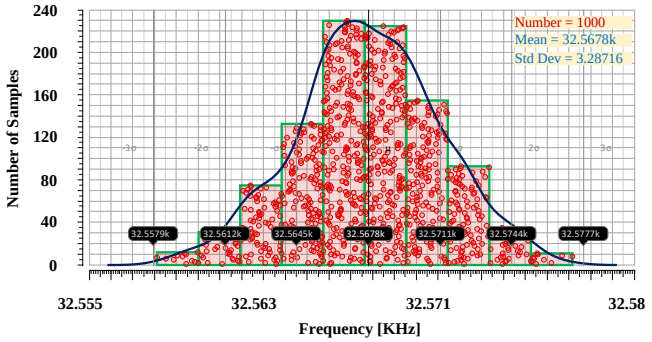


Fig. 11: The frequency response of the proposed filter for the bias voltage presented in Table 3.

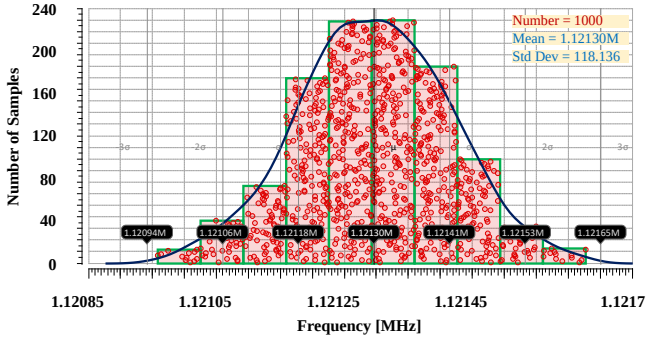
In order to investigate the effect of capacitor tolerance in the cutoff frequencies of the proposed filter, a Monte Carlo analysis is run. As shown in Fig. 12, the error created in the cut-off frequencies of the proposed filter is not significant for 2% deviation in the capacitance of the used capacitors. Table 4 provides the comparison of the proposed filter with previous reported band-pass filters. Among the reported band-pass filters, the proposed fourth-order band-pass filter exhibits a competitive feature despite the use of fewer amplifiers and lower capacitance.

4. CONCLUSIONS

The OTA-C fourth-order band-pass filter, which has the ability to adjust the bandwidth, was designed with 180 nm CMOS technology and simulated using C.a.d.e.n.c.e software. Using the low-pass and high-pass filters, the proposed band-pass filter is designed that can be used as an anti-aliasing filter. In order to utilize the proposed anti-aliasing in the front-end of the ADC that is used in ADSL technologies, it is possible to adjust the lower and upper cut-off frequencies of the filter using two bias voltages. The simulation results showed that by adjusting the bias voltages, the bandwidth of the proposed filter can be tuned between 1.1 and 2.2 MHz. Also, the power consumption of the proposed filter is 327 µW at supply voltage of 1.8V. The total capacitance and the number of trans-conductance amplifiers used in the proposed filter are 20 pF and 8, respectively.



(a)



(b)

Fig. 12: Histograms of Monte Carlo analysis on the proposed filter (a) lower cut-off frequency (b) upper cut-off frequency.

Table 4: Comparison of proposed filter with the reported works.

	This work	[15]	[16]	[17]	[18]
Technology (µm)	0.18	0.18	0.18	0.18	0.13
Filter type	Gm-C	Gm-C	Gm-C	Gm-C	Gm-C
Voltage (V)	1.8	1.8	1.2	1.8	0.6
Filter Order	4	8	2	5	1
Number of Amplifire	8	16	5	10	6
Central frequency (MHz)	1.12	0.5	0.13	1.17	2
Sum of Capacitance (pF)	20	88	24	45	30
Power consumption (µW)	327	448	150	954	261

CREDIT AUTHORSHIP CONTRIBUTION STATEMENT

Mohsen Ghaemmaghami: Formal analysis, Investigation, Investigation, Software, Roles/Writing - original draft. **Shahbaz Reyhani:** Methodology**,** Supervision, Validation, Writing - review & editing

DECLARATION OF COMPETING INTEREST

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper. The ethical issues; including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, redundancy has been completely observed by the authors.

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BIOGRAPHY



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Shahbaz Reyhani was born in 1969. He received his B.Sc., M.Sc. and Ph.D. degree in electronic engineering from university of Guilan, Shiraz university and Shahid Beheshti university, respectively, in Iran. Dr. Reyhani is an assistant professor with department of electrical engineering, university of Guilan, Rasht, Iran. His research interests include low-power integrated circuits, data converters, digital systems and neural networks.

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