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Research Article

A Feedforward Active Gate Voltage Control Method for SiC MOSFET Driving

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Abstract: A new active gate drive for Silicon carbide (SiC) metal–oxide–semiconductor field-effect transistor (MOSFET) is proposed in this paper. The SiC MOSFET as an attractive replacement for insulated gate bipolar transistor (IGBT) has been regarded in many high power density converters. The proposed driver is based on a feedforward control method. This simple analog gate driver (GD) improves switching transient with minimum undesirable effect on the efficiency. This paper involves the entire switching condition (turn on/off), and the GD is applied to the SiC base technology of MOSFET. To evaluate the performance of the proposed GD, it will be compared with a conventional gate driver. The presented GD is validated by experimental tests. All the evaluations are carried out in a hard switching condition and at high-frequency operation.

Keywords: Active gate driver (AGD), SiC MOSFET, switching condition, feedforward control.

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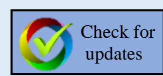


1. INTRODUCTION

Conventional IGBTs are conventional switches in the structure of the power converters. However, because of some weak points such as operation in low-speed switching and low-temperature condition, the studies have been driven to silicon carbide (SiC) technology. SiC technology in power switches has emerged as a serious alternative to overcome the disadvantages of Si-switches. SiC device has some advantages such as higher operating frequency and temperature and lower on-resistance due to its bandgap and unipolar nature [1-2]. Moreover, due to its fast switching behaviour and shorter switching time, a better switching efficiency can be expected. In order to gain as efficiently as possible, engineers try to switch as fast as possible. However, the high speed switching in SiC MOSFETs increases the electromagnetic interference (EMI) emission. Therefore, the existing trade-off between efficiency improvement and EMI reduction through switching control brings a challenge in the gate driver designing. In addition, the SiC MOSFET normally has large input capacitance and higher threshold voltage, therefore more complex and sensitive driver is needed [3].

Several gate drivers (GDs) have been presented to improve the mentioned trade-off between fast switching and EMI [4-8]. However, most of them have been assigned to Si-MOSFET or IGBT applications. Also, mainly they can be categorized in the closed-loop controller. Typically such controllers are effective and comprehensive for GDs, but in general, they increase the complexity of the GD's circuit. Therefore, some of the presented approaches are not attractive solutions for industrial. Moreover, in high-frequency operation rates, when SiC MOSFET is under hard switching condition; the advent of EMI problem is possible. Hence, designing proper GD for SiC MOSFETs has significant importance.

1.1. Overview of Gate Drivers for Power Devices

In order to enhance power density in switch-mode applications, operation at high switching frequency is necessary due to reducing the size of its passive component as well as it reduces the size of the heatsink. Thereby, the operation of IGBT is limited at the low switching frequencies (<20 kHz) [9]. However, in high speed switches the transition rates of current and voltage (*di/dt* and *dv/dt* respectively) get higher values. Also, parasitic inductance results some problematic oscillations and overshoots in current and voltage waveforms [10]. Changing the gate resistor R_g is known as a conventional solution [11-12]. Although the overshoot suppression can be achieved by high R_g value. However, the id and V_{ds} both get lower slopes which cause to increase switching times. As a result, the increased R_g

sacrifices additional switching losses. Another conventional driving technique is the use of an external gate-source capacitance (C_{gs}) in the GD circuit [13]. However, it increases the input capacitance (C_{ies}). This technique is used for IGBT's gate drivers due to roughly better efficiency (compared to the method of solely R_g increasing). Nevertheless, the gate capacitance is a parasitic element which potentially provokes transients and it can create some parasitic problems such as imposing the stress and crosstalk problem [14-15]. As a result, this may not be a favorable solution for SiC MOSFET applications which typically has large input capacitance. To improve the existing trade-off between switching loss, stress and EMI; diverse approaches have been proposed such as applying snubber circuits in Si and SiC devices [16-17] active gate voltage controlling [18] active gate current driving [19] resonant gate drivers [16, 20], etc. All mentioned techniques could be used for driving SiC MOSFETs. Although, these GDs can minimize stress from the power device, however, these deal with more complexity or more cost and more switching losses. The control of GDs is not the single possible way for EMI reduction, rather with using a better design of PCB layout the parasitic (stray) inductances can be reduced, and consequently we will have less EMI problems.

1.2. SiC MOSFET Gate Drivers

The SiC MOSFETs are widely employed in power converters due to its advantages. This switching technology inherently has lower trans-conductance compared to Si-MOSFETs or IGBTs. Thus, higher orders of gate-source voltage are required for switching-on. Also, the gate-source voltage pulse is commonly asymmetrical. Therefore, different values of Rg should be used in their GDs [21]. Conventionally, two different gate resistance is used in the drive circuit for controlling each turn path. This common driver controls both turn-on and turn-off paths separately. A gate boost circuit was introduced for SiC MOSFET driving in [22] which had reduced the switching losses, however, the transient and overshoots had not been reduced. The same technique is presented in [23] as well. Many studies for controlling *di/dt* and *dv/dt* transition by closed-loop control method have been reported [23-26]. Such controllers have been allocated to guarantee the safe operation of MOS-gate switches under different and variable loads. However, they increase the complexity of the driver's circuit.

According to the presented overview, most of the offered approached are related to efficiency improvement and for solving some other issues such as EMI reduction, overshoot suppression, stability improvement etc. mainly the presented solutions have fallen in the complex closed-loop GD controllers. This paper presents a simple control method for driving SiC MOSFETs. The control concept is based on a feed-forward controller. The effective performance of the controller beside its simple structure is the main advantage of this GD. The purpose is the switching transient improvement with a minimum undesirable effect on efficiency. In the next section, the operation of SiC MOSFET and the principles of new GD are presented.

2. Active Gate Driver

2.1. Principles of Proposed Controller

The test circuit is represented in Fig. 1. The controller is applied into the gate circuit. The profile of Vgg voltage signal is changed by the controller and it is delivered to the gate port of MOSFET. In order to test in a hard-switching condition, the load is highly inductive.

The schematic of the proposed controller is depicted in Fig. 2. Since the SiC MOSFET meets several intervals during the switching conditions, controller changes the profile of gate signal during MOSFET's active region (Fig. 3a shows these intervals). The modification process of gate signal has been demonstrated in Fig. 3b. The turn-on is initiated at t_0, and step voltage (from $-V_{EE}$ to $+V_{CC}$) is applied to the gate. As shown in Fig. 2, each switching state is separated from the other by diodes for individual controlling. The positive side of voltage signal is driven by d_1 and the d_2 conducts its negative for turn-on and turn-off controlling respectively. Both control paths have same structure and operate based on same concept.

However, the required parameters should be defined according to each switching condition. In both cases, the controller gets a step voltage value (ΔV_g) according to (1) from the input. Depending on the suppression rate of overshoot at each swathing state, a portion of the input value is given to the corresponding control path. K_i and K_v represent these coefficients for turn-on and turn-off controlling respectively.

In each switching condition, weakened signal with a negative coefficient is summed with the same positive signal

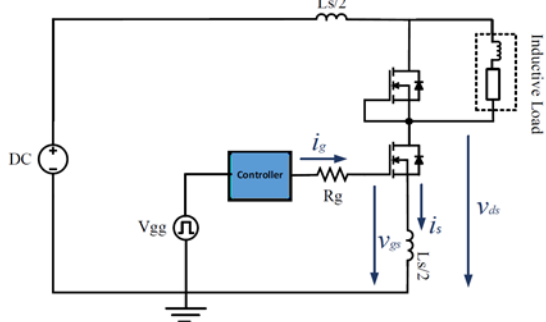


Fig. 1: Schematic of test circuit.

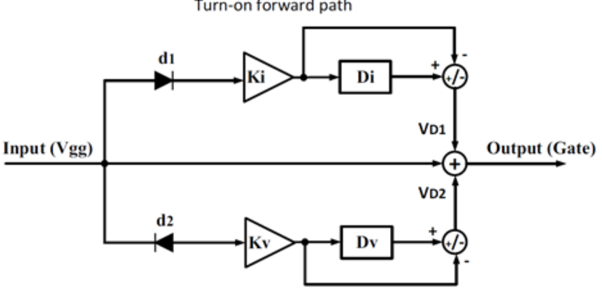
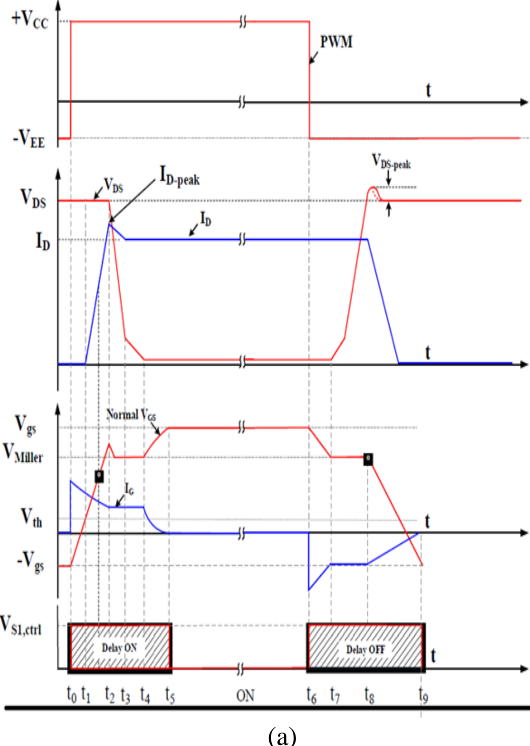
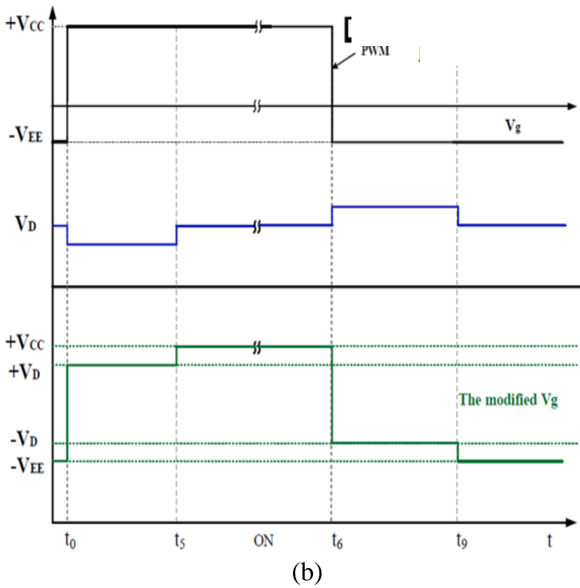


Fig. 2: Block diagram of the proposed feedforward controller.



(a)



(b)

Fig. 3: (a) The transient behavior of MOSFET switching, and (b) controller performance for Vg modification.

that has a delay. These delays are created by blocks D_i and D_v. The applied D_i delay covers whole turn-on ($t_0 < t < t_5$) and D_v covers turn-off ($t_6 < t < t_9$) intervals. The resultant voltage signal is called V_D here. Finally, the original V_{gg} signal after summing with V_{D1} and V_{D2} results modified V_g signal which is applied on gate port for driving MOSFET. The modified V_g affects to the current transient while turn-on condition and as well as to the dynamic of voltage during turn-off condition.

$$\Delta V_g = V_{cc} - V_{EE} \tag{1}$$

According to what has been presented in [27], with a little approximation the current and voltage transitions may be defined as (2) and (3), which both depend on a different voltage value between $V_g(+/–)$ to $V_{gs}(th)$. This differential voltage value affects to the injected gate current i_g in each switching state. Thereby, the used technique can be effective to control of both current and voltage transitions.

$$\frac{d_{id}}{dt} = g_m \cdot \frac{V_{cc} - V_{gs}(th) - \dfrac{id}{2 \cdot g_m}}{C_{iss} \cdot Rg} \tag{2}$$

$$\frac{dv_{DS}}{\text{dt}} = \frac{V_{EE} + V_{gs(plateau)}}{C_{gd} \cdot R_g} \tag{3}$$

In (2), g_m is the trans-conductance and $C_{iss}= C_{gs}+C_{gd}$ is the input capacitance of the SiC MOSFET. All details about the switching process of the MOSFET is fairly well demonstrated in [10]. Here, we present the performance of the new gate driver for controlling di_d/dt and dv_{ds}/dt rates.

2.2. Parameters and Limitations

For tuning the controller in each switching state two parameters are necessary. K_i coefficient and the D_i delay for turn-on and K_v coefficient and the D_v delay for turn-off. In the case of delays, these parameters can be determined based on application note or experimental observations. As already mentioned, the delay time must cover whole active region times. Because of the time difference between switching on and off, two individual delays have been considered for corresponding states as shown in Fig. 2. It should be noted that the margin determination for delays is not a delicate factor. Because after finishing D_i or D_v delay, the modified V_g returns to its original value when MOSFET is in the saturation (steady state) region. For this reason, the delay time could be defined much longer than switching time. The K coefficient determines V_D voltage value (see Fig. 3b and (5)) or in other word, it determines the ΔV_g voltage value while controlling time. As a result, the injected gate current and then switching transient will get effect by that. V_D is the reduced voltage level during turn on/off. Since the SiC MOSFETs driving is asymmetric and the absolute value of V_{EE} is smaller than V_{CC}, thus the change domain of the V_{gg} for each switching state must be determined individually. For turn-on condition K_i coefficient can be obtained by the following equations.

$$V_{gs}, th < \sigma_1 < V_{cc} \tag{4}$$

$$V_D^+ = V_{cc} - \sigma_1 \tag{5}$$

$$\Delta V_{m1} = V_D^+ - V_{EE} \tag{6}$$

$$K_i = 1 - \left(\frac{\Delta Vm1}{\Delta V_g}\right) \tag{7}$$

As well as for turn-off condition, K_v coefficient can be defined as:

$$V_{EE} < \sigma_2 < 0 \tag{8}$$

$$V_D^- = V_{EE} - \sigma_2 \tag{9}$$

$$\Delta V_{m2} = V_{cc} - V_D^- \tag{10}$$

$$K_v = 1 - \left(\frac{\Delta V_{m2}}{\Delta V_g}\right) \tag{11}$$

In the mentioned equations σ_1 and σ_2 are variable factors which should be selected according to the desired di_d/dt and dV_{ds}/dt rates respectively with considering the limitations presente in (4) and (8). For turn-on condition the modified V_g has been limited by $V_{gs,th}$ and for turn-off condition it has been limited by zero. Accordingly, smaller ΔV_m has higher impact on the switching transient and oscillations suppression.

2.3. Controller Tuning

According to the presented method, the level of applied intermediate voltages and their time duration should be determined. The influence of each control parameter on the switching transient behaviour is explained here. Also, the optimal interval values for each switching condition should be determined.

2.3.1. Tuning for turn-on

Based on what expressed in previous section, Ki coefficient determines the level of intermediate voltage which can be reduced up to MOSFET's threshold voltage. As a result, the applied intermediate voltage affects to did/dt and current overshoot at turn-on. The time duration of intermediate voltage is another consideration that must be long enough to cover turn-on active region. In this case study, 3 µs has been considered for Di. In order to realize which level of reduced gate voltage provides a desirable did/dt and current overshoot, the corresponding MOSFET is tested by different intermediate voltage values. Fig. 4 shows the effect of controller on MOSFET behaviour at turn-on.

2.3.2. Tuning for turn-off

Also, the voltage transition (dv/dt) and overshoot ($V_{DS\text{-}peak}$) are being affected by intermediate voltage while turn off condition (according to (3)). The resultant intermediate gate voltage through K_v and its consequence on MOSFET behaviour at turn-off has been reflected in Fig. 5. In this controlling stage, D_v is 2 µs which covers whole transient behaviour of MOSFET while turn-off with considering worst case.

3. Test Condition

Experimental tests evaluate the performance of the proposed gate driver. The test circuit is a standard clamped-inductive circuit which is depicted in Fig. 1. The driving power SiC MOSFET and the clamped SiC MOSFET both are from a same type (SCT2080KE). The parasitic inductance (LS) which comes from the loop of the PCB and power devices is 120 nH. The load current is 6 A, and the value of L in load is 330 µH. A square signal with 50% of duty cycle and frequency at 100 kHz has been applied to the input. The voltage of dc-bus is 400 V and the V_{gg} supply for original gate driver is −5/+18 V. The applied gate resistor (R_g) for turning-on is 33 ohms and for turning-off is 46 ohms. The experimental waveforms have been captured by a Tektronix MSO 4054 (500 MHz) digital oscilloscope. The insulators and the safety instruments for protection are not demonstrated here.

3.1. Optimized Tuning

The product of multiplication of the drain-source voltage $V_{dsi}(t)$ to output current $I_d(t)$ during the switching time results

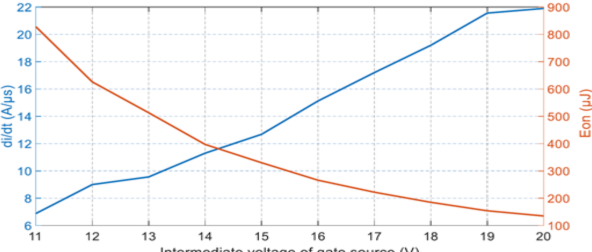


Fig. 4: The effect of intermediate gate-voltage levels on the peak value of current transient and di_d/dt while turn-on control domain.

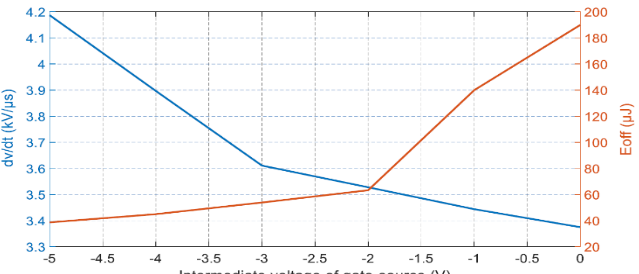


Fig. 5: The effect of intermediate gate-voltage levels on voltage transition and voltage overshoot in turn-off control domain.

corresponding switching loss. The lost energy while turn-on and turn-off can be calculated from (12) and (13), respectively. Accordingly, to reach an optimized design, the effect of K_i and K_v on switching loss and peak value of oscillations are evaluated.

$$E_{on} = \int_{t_0}^{t_5} v_{ds(t)} \times i_{d\,(t)}\ \mathrm{dt} \tag{12}$$

$$E_{off} = \int_{t_6}^{t_9} v_{ds(t)} \times i_{d\,(t)}\ dt \tag{13}$$

First, each one of the switching losses and peak values of current transient (at turn-on) and voltage overshoot (at turn-off) must be normalized as below equations.

$$\alpha = \frac{E_{on}}{E_{min,on}} \tag{14}$$

$$\beta = \frac{E_{off}}{E_{min,off}} \tag{15}$$

In this analysis, the minimum value of switching loss (E_{min}) is assumed when the minimum possible value of R_g has been used. This value for each switching condition is 6.3 Ω. Also, in this condition the maximum peak value of current transient ($i_{d,max,peak}$) and maximum voltage overshoot ($V_{ds,max,ov}$) can be measured.

$$\gamma = \frac{di_d/dt}{d_{id}/dt - max} \tag{16}$$

$$\delta = \frac{dv_{ds}/dt}{dv_{ds}/dt - max} \tag{17}$$

α and γ present the normalized values of the lost energy and peak value of current oscillations at turn-on condition respectively. Also, β and δ represent the normalized values of the lost energy and voltage overshoot at turn-off condition

respectively. With these assumptions, the optimal intermediate gate voltages for each switching state can be obtained. Fig. 6 and Fig. 7 show these optimal intermediate gate-source voltages.

To realize the effect of V_{GS} value on the transient behaviour of switch while turning-on equation (18) represents the relation of current peak normalized value (see (16)) to the normalized value of lost energy (see (14)) for a specific VGS value at turn-on condition. Also, in the same way it can be realized for turning-off condition by (19).

The test results base on (18) have been reflected in Table 1 and for turn-off condition have been reflected in Table 2. Then, the highest value of γ/α column expresses the highest impact of V_{GS} value or in other word it belongs to optimum value of V_{GS}.

$$V_{GS_{on}} = \left|\frac{\gamma_n}{\alpha_n}\right|_{max} \tag{18}$$

$$V_{GS_{off}} = \left|\frac{\delta i}{\beta i}\right|_{max} \tag{19}$$

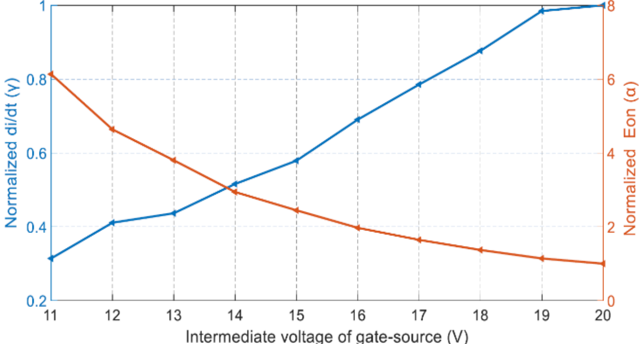


Fig. 6: Optimal intermediate voltage for gate-source (*V*) at turn-on.

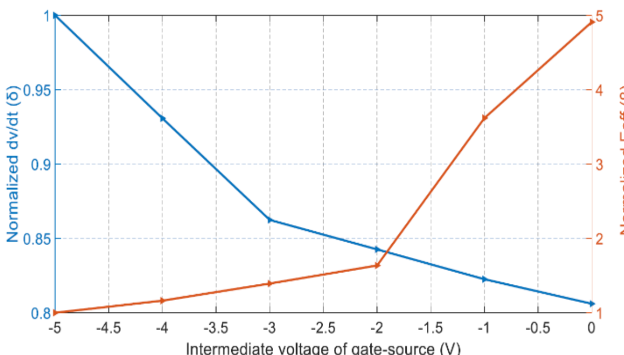


Fig. 7: Optimal intermediate voltage for gate-source (V) at turn-off.

Table 3 shows the optimal setting at both switching states and corresponding values. Through original GD, SiC MOSFET has been driving with V_g= +20/-5 V and the implemented external gate resistor (R_g) is valid for the new GD as well. Though defined coefficients, Ki delivers V_{D+} = 18V to the gate for switching-on and by K_v it gets V_{D-} = -4V while turn-off state.

4. Experimental Validation

The proposed GD is validated by experimental tests. In order to evaluate the performance of new GD, the transient behaviour of the MOSFET in both with original GD and with proposed GD are compared with together.

4.1. The Test Results

The profile of output parameters (i_d and V_{DS}) of MOSFET when it is driven by original GD are demonstrated in Fig. 8. Then in next figure, for a closer look, the switching behaviour of MOSFET driven by new GD is zoomed in different tuning conditions.

As can be seen in Fig. 9, the overshoot value in output current and corresponding oscillations can be suppressed by applying different K_i. The biggest suppression rate belongs to which has smallest ΔV_{m1} (see (6) and Fig. 3). However, the optimized value (V_{D+} = 18V and V_{D-} = -4V) for driving is compared with original gate driver. Fig. 10 and Fig. 11 represent the i_d current waveform while turning on and off conditions.

Although the proposed GD may suppresses the overshoot up to 5.2 A, however, the optimized tuning condition the overshoot can be reduced up to 5.5 A. In this tuning condition,

Table 1: Optimal VGS value in turn-on condition.

n	V_{GS}	γ	α	γ/α
1	19	0.0155	0.141	0.1099
2	18	0.01078	0.229	0.4707
3	17	0.0913	0.274	0.3332
4	16	0.095	0.326	0.2914
5	15	0.111	0.474	0.2341
6	14	0.063	0.497	0.1267

Table 2: Optimal VGS value in turn-off condition.

i	V_{GS}	γ	α	γ/α
1	-4	0.0693	0.163	0.425
2	-3	0.0683	0.23	0.297
3	-2	0.0198	0.243	0.0815

Table 3: The controller tuning parameters.

	P	Value	P	Value	$E_{on}(\mu J)$	$E_{off}(\mu J)$	$E_{min}(\mu J)$	$id, \max(A)$	$Vds, max, or(V)$
$Turn-on$	K_i	0.122	α	1.52	190	-	125	6.6	-
	D_i	3 µs	γ	0.86					
$Turn-off$	K_v	0.1	β	1.18	-	46	39	-	580
	D_v	2 µs	δ	0.93					

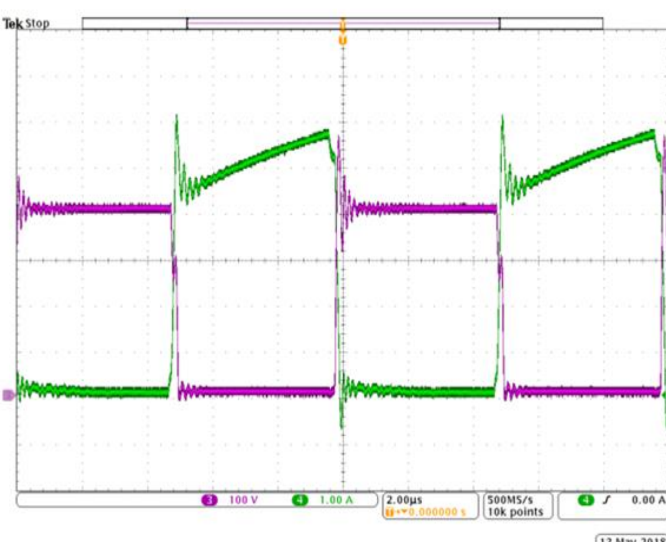


Fig. 8: Output voltage and current of MOSFET driven by original GD.

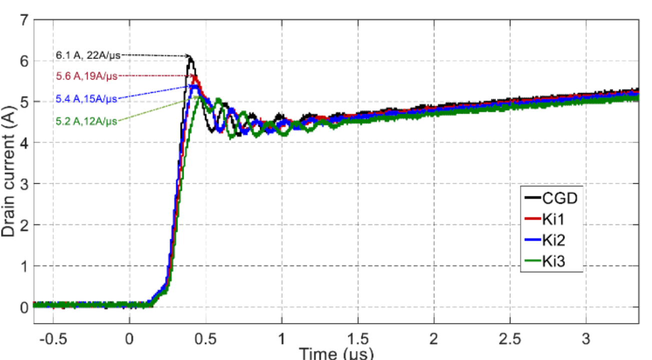


Fig. 9: Zoomed view of drain current with different K_i.

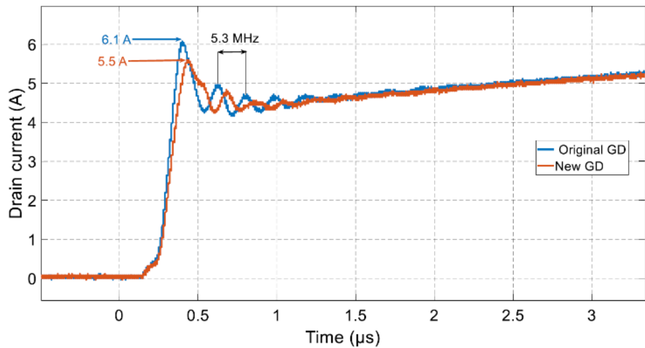


Fig. 10: Drain current with new GD (optimal tuning value) and original GD at turning-on.

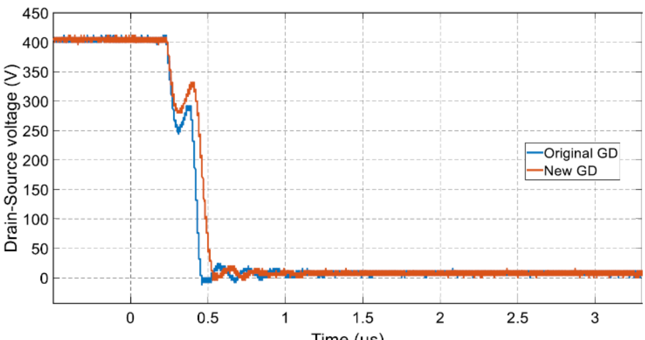


Fig. 11: Drain current with new GD (optimal tuning value) and original GD at turning-off.

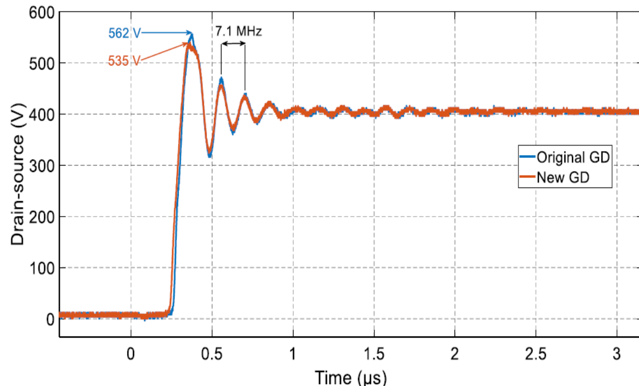


Fig. 12: Drain-Source voltage with new GD (optimal tuning value) and original GD at turning-on.

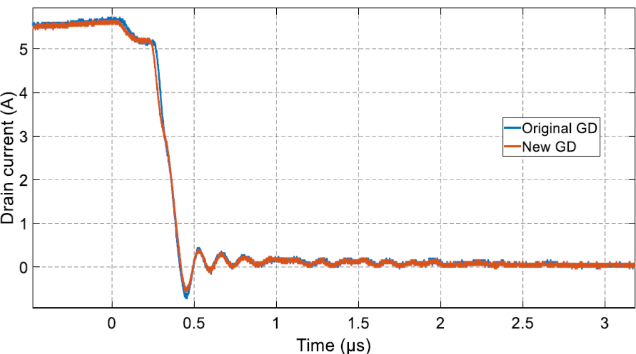


Fig. 13: Drain-Source voltage with new GD (optimal tuning value) and original GD at turning-off.

the slope of the current (di_d/dt) in fundamental frequency (100 KHz) ten times has been increased compare to its maximum value. Also the current fluctuation in switching-on condition with 5.3 MHz (see Fig. 10) highly has been removed which both manners help to eliminate EMI problem from switch mode power supplies.

This comparison can be carried out in the case of drain-source voltage as well. Fig. 12 and Fig. 13 demonstrate the output voltage profiles with original and new GDs in both switching condition.

The obtained results show that output voltage at turn-off condition gets minimum effect from applied control method.

4.2. Performance Index

Based on previous subsection, the experimental setup of the gate driver for both switching states has developed. In order to observe the effect of the applied GD, an analytical test between new GD and original GD (with minimum $R_{g,ext}$ values) has been carried out. The purpose of this comparison is the evaluation of transient behaviour during the operation of new GD and the CGD. Another criteria in this analysis is the comparison of the switching losses between these GDs. The change of gate resistor ($R_{g,ext}$) is known as a conventional driver for MOS-channel switches [27-28]. So, as a conventional solution, $R_{g,ext}$ is increased up to 15 Ω (for turning on) and 22 Ω (for turning off) to achieve the same level of overshoot suppression in current and voltage that new GD presents in its operation. In this condition the switching losses of both GDs can be calculated according to (12) and (13). The results have reflected in Table 4.

Table 4: The performance index.

Gate driver	I_d (A) overshoot	Voltage overshoot (V)	E_{on} (µJ)	E_{off} (µJ)	di_d/dt (A/µs)	dv_{ds}/dt (KV/µs)
Original gate driver	6.1	562	125	39	22	4.2
New gate driver	5.5	535	190	46	19.2	3.9
CGD, $R_{g,on}$=15 Ω $R_{g,off}$=22 Ω	5.5	535	212	50	18.5	3.6

5. Conclusion

Based on the obtained results, the new active voltage gate driver has improved transient behavior of the SiC MOSFET in both switching condition. Although this technique mostly improves the switching in turn-on condition, however it has better performance compared to CGD. In this study, we tried to use an optimized gate drive for switching in both switching states. Applying the proposed feedforward controller on SiC technology MOSFETs, optimal tuning of active voltage GD and evaluation of this GD by performance index were the important topics of this study.

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CRediT Authorship Contribution Statement

Hamidreza Ghorbani: Conceptualization, Data curation, Formal analysis, Funding acquisition, Investigation, Methodology, Software, Validation, Visualization, Writing - original draft. **Jose Luis Romeral Martinez:** Conceptualization, Supervision, Validation, Writing - review & editing.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper. The ethical issues; including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, redundancy has been completely observed by the authors.

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