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Research Article

Design of a Tuneable Low-Power Band-Stop Filter for the Elimination of 50-Hz Power-Line Noise

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Abstract: The electrocardiogram is affected by various noises among which one of the most important ones is 50-Hz power-line noise. On the other hand, it is necessary to use a battery in portable devices, so it is necessary to use low-power consumption circuits. Therefore, one of the challenges ahead when designing this type of device is the use of energy-saving filters that can integrate devices and attenuate unwanted signals properly. This paper presents a low-power tuneable sixth-order band-stop filter that does not need off-chip capacitors. The filter structure is based on operational transconductance amplifiers and integrated capacitors. Also, it is possible to change the central attenuation frequency of the proposed filter using the bias voltage of the transconductance amplifiers. The proposed band-stop filter is designed and simulated in 180-nm CMOS technology at the transistor level. The simulation results show that the proposed filter

can attenuate unwanted signals at 50 Hz by 102 dB while the maximum capacitance used in the filter is 54 pF. The power

Keywords: Electrocardiogram, low-power filter, band-stop filter, notch filter, power-line noise.

consumption of the proposed band-stop filter is 13.1 nW at a supply voltage of 1.8 V.

Article history

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1. Introduction

The electrocardiogram is one of the most common devices in medical applications to measure electrical signals related to heart patients [1]. Portable electrocardiogram devices enable physicians to measure and remotely control patient conditions, which is essential given the advancement of technology and the conditions of some patients [1-3].

One of the factors that can disrupt the operation of the electrocardiogram device is a variety of noises among which one of the most important ones is power-line noise that occurs at a frequency of 50 or 60 Hz. This unwanted signal interferes with the original signal and makes the process of measuring and diagnosing patients' problems difficult [4-6].

Band-stop or notch filters, which are analog and suitable for real-time processing, are used to eliminate power-line noise. Unlike digital filters and adaptive filters, analog filters do not require high-speed processors [2-8].

Various structures of analog filters have been used to eliminate power-line noise [8]. Due to the high sensitivity of electrocardiogram devices, the circuits used in these devices must have high accuracy, low power, proper attenuation of

noise, and also the ability to integrate. Therefore, the bandstop filter used in electrocardiogram devices must also have these specifications [1-3].

Portable electrocardiogram devices are no exception to this rule. In some studies, the use of circuits with high power consumption and the use of resistors and capacitors with high values in the filter do not make it possible to integrate these circuits [9-13].

This article presents a tuneable band-stop filter that can attenuate the annoying 50-Hz signal of the power line by 102 dB. The proposed filter outperforms other filters owing to its very low power consumption (nano-watts), good attenuation, simple structure, small capacitor, and no resistor.

2. THE STRUCTURE OF THE SECOND-ORDER OTA-C BAND-STOP FILTER

The proposed band-stop or notch filter uses three stages of second-order band-stop filters. The second-order notch filter uses only operational transconductance amplifiers (OTA) and capacitors and is based on the OTA-C structure. Fig. 1 shows the second-order OTA-C band-stop filter circuit.

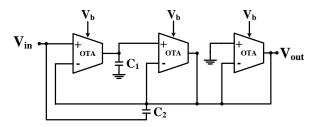


Fig. 1: The second-order band-stop filter, used in the proposed filter.

second OTA-C notch filter three uses transconductance amplifiers. The proposed filter transfer function is shown in (1).

$$TF = \frac{S^2 C_1 C_2 + g_{m1} g_{m2}}{S^2 C_1 C_2 + S g_{m2} C_1 + g_{m1} g_{m2}} \tag{1}$$

where C_1 and C_2 are the capacitors used in the circuit, and g_{m1} , g_{m2}, and g_{m3} are the first, second, and third transconductance amplifiers in the band-stop filter. The cut-off frequency (ω_0) and the quality factor (Q) of the filter are obtained by (2) and

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{c_1c_2}} \tag{2}$$

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{c_1 c_2}}$$

$$Q = \left(\frac{\sqrt{g_{m1}g_{m2}}}{g_{m3}}\right) \sqrt{\frac{c_2}{c_1}}$$

$$(2)$$

By changing the transconductance of the amplifiers according to (2), the cut-off frequency of the filter can be changed, which is possible by changing the amount of bias voltage (V_b) in the amplifier, which is described in the next section.

Although the proposed band-stop filter is used to attenuate 50-Hz noise by changing the bias voltage between 0.12 and 0.2 V, the central frequency of the filter can be changed approximately between 4 and 100 Hz for C_I =16pF and C_2 =2pF. Table 1 compares the calculated and simulated values of the transconductance for different central frequencies of the filter. The bias voltages of the OTAs in the proposed filter are the same. The higher bias voltages increase the central frequency of the filter, but since the amplifier exits from the sub-threshold region, the attenuation of the filter decreases and its power consumption also increases. Table 2 compares the calculated transconductance and quality factor with the simulated ones for central frequency of 50 Hz.

Fig. 2 shows the frequency response of the proposed second-order notch filter.

2.1. The Operational Transconductance Amplifier

The transconductance amplifier circuit used in the proposed filter stages shown in Fig. 3.

The proposed differential amplifier has a gain of 90 dB, a bandwidth of 5.7 MHz, a phase margin of 69°, and a common-mode rejection ratio (CMRR) of 110 dB. The inputs of this amplifier are PMOS type, which is not sensitive to flicker and offset noise. The gain and phase characteristics of the proposed transconductance amplifier are shown in Fig. 4.

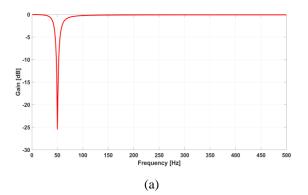
By changing the bias voltage (V_b) , the amount of transconductance (g_m) will change.

Table 1: The comparison of calculated g_m with simulated values. The calculated g_m is obtained using existing central frequency for C_1 =16pF and C_2 =2pF.

$V_{bias}(V)$	fo (Hz)	$g_{m \ (calc.)}(\mathrm{nS})$	$g_{m(simu.)}(nS)$
0.125	4.1	0.146	0.346
0.13	8.07	0.287	0.434
0.14	21.47	0.763	0.670
0.15	29.6	1.05	0.922
0.16	39.17	1.39	1.28
0.17	50.93	1.81	1.78
0.18	65.46	2.33	2.47
0.19	83.56	2.97	3.40
0.20	105.68	3.76	4.66

Table 2: The comparison of calculated parameters of the second-order 50-Hz notch filter with the simulated values.

Parameters for central	Filter Specification		
frequency of 50 Hz	Calculation	Simulation	
g_m	1.78nS	1.81nS	
Q	2.82	3.19	



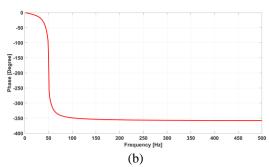


Fig. 2: The frequency response of the proposed secondorder band-stop filter including (a) gain, and (b) phase.

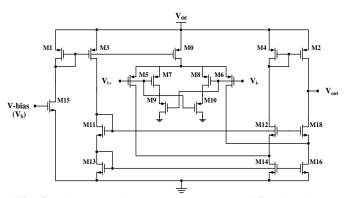
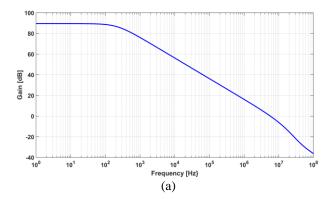


Fig. 3: The proposed transconductance amplifier circuit.



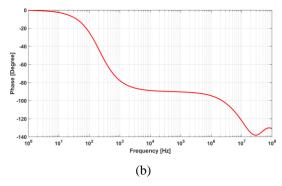


Fig. 4: The frequency response of the proposed operational transconductance amplifier for V_b =0.9V including (a) gain and (b) phase.

The OTA is designed by the following procedure. 1) The current of each branch is determined from the slew rate requirements. 2) The transconductance of the input transistors is determined from the GBW.

$$g_m = 2\pi \times GBW \times C_L \tag{4}$$

3) The size of the input transistors is obtained by

$$\left(\frac{W}{L}\right) = \frac{\left(g_m\right)^2}{2\mu C_{ox} \times I_D} \tag{5}$$

4) For other transistors, V_{DSAT} is at least 50-200mV. When V_{DSAT} is determined, the size of each transistor is set using

$$\left(\frac{W}{L}\right) = \frac{2I_D}{\mu C_{ox} \times V_{DSAT}^2} \tag{6}$$

Based on the above-mentioned designing procedure, the single-stage OTA is designed. Then, the W/L of transistors are obtained using a sizing procedure (based on the trade-off method) performed by a simulation tool in CMOS 180nm technology. Table 3 shows the design results of the proposed OTA.

The power consumption of the proposed OTA with a bias voltage of 0.9V and a power supply of 1.8V is 69 μ W. To use this OTA in the proposed filter, the bias voltage must be reduced to 0.17V, which will reach a power consumption of 1.4 nW. In this case, the dc gain will be equal to 25 dB.

3. THE PROPOSED LOW-POWER TUNEABLE BAND-STOP FILTER STRUCTURE

The proposed structure of the sixth-order low-power tuneable band-stop filter is shown in Fig. 5.

Table 3. The parameters of transistors in the proposed OTA

Transistor	W (µm)	L (µm)	$I_{D}\left(\mu A\right)$	$g_{m}\left(\mu S\right)$	$V_{DSAT}\left(mV\right)$
M_0	28	0.18	9.6	82	120
\mathbf{M}_1	28	0.18	10	213	57
M_3	28	0.18	10	210	60
M_2 - M_4	28	0.18	4.3	98	50
M_5 - M_6	14	0.18	3.3	72	52
M_7 - M_8	14	0.18	1.5	31	51
M_9 - M_{10}	14	0.18	1.5	33	47
M_{11}	10	2	10	148	128
M_{12} - M_{18}	2.5	2	4.3	53	159
M_{13}	10	2	10	147	126
M_{14} - M_{16}	7.5	2	7.7	112	126
M_{15}	0.61	2	10	40	440

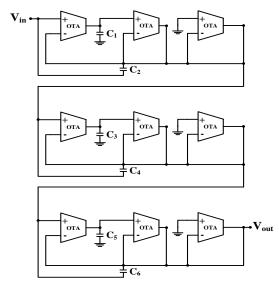


Fig. 5: The structure of the proposed sixth-order band-stop

In each stage, there are three transconductance amplifiers that can be tuned by changing the bias voltage. For a central frequency of 50 Hz, the values of the capacitors used are C_1 = $C_3 = C_5 = 16$ pF and $C_2 = C_4 = C_6 = 2$ pF, and the bias voltage is $V_b = 170$ mV.

4. SIMULATION RESULTS

The proposed filter was designed and simulated in 180 nm technology at the transistor level. The frequency response of the filter is shown in Fig. 6.

As can be seen, the proposed filter attenuates the 50-Hz signal by 102 dB. This filter is tuneable and the central attenuation frequency can be changed by adjusting the g_m values of the transconductance amplifiers.

Fig. 7 shows the frequency response of the proposed filter output for schematic and post-layout simulation. Due to the tuneable nature of the filter, the central frequency in the post-layout circuit can be shifted by changing the input bias voltage, which will eliminate the negative effect of parasitic components on the filter performance.

This feature also makes the proposed filter compatible to eliminate the power-line noise in some countries with a frequency of 60 Hz. Also, the low power consumption of 13.1 nW and integrability can be considered the advantages of the proposed filter.

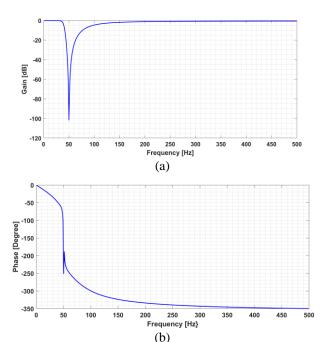


Fig. 6: The frequency response of the proposed sixth-order band-stop filter including (a) gain, and (b) phase.

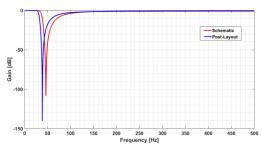


Fig. 7: The frequency response for schematic and post-layout simulation of the proposed sixth-order band-stop filter

The effect of the capacitance deviation on the central frequency of the proposed sixth-order band-stop filter is investigated using Monte Carlo analysis. As shown in Fig. 8, the error created in the central frequency of the filter is not significant for 2% deviation in the capacitance of the capacitors Also, separate simulations were performed for different corners. Their frequency responses are shown in Fig. 9. Considering the capability of the proposed filter, the central frequency of the band-stop filter can be set to the desired frequency by changing the input bias voltage.

The layout of the proposed sixth-order band-stop filter is shown in Fig. 10. The dimensions of the layout are 459 μM by 303 μM .

The proposed filter is compared with the previously reported works. As shown in Table 4, this filter is superior to the reported filters in terms of low power consumption, low capacitance, high attenuation rate, and lack of resistance.

5. CONCLUSION

The tuneable sixth-order band-stop filter to eliminate power-line noise for use in portable electrocardiograms is designed and simulated in 180 nm CMOS technology. The

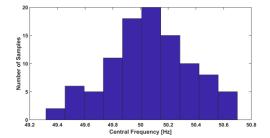


Fig. 8: The histogram of Monte Carlo analysis on the proposed filter.

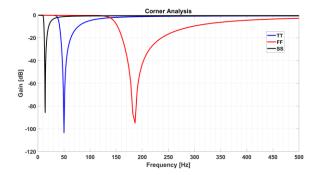


Fig. 9: The frequency response of the proposed filter for different corner simulations.

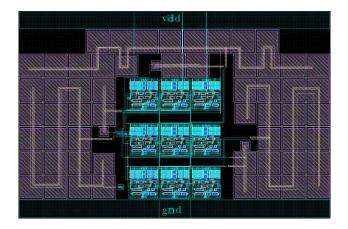


Fig. 10: The layout of the proposed sixth-order band-stop filter.

proposed filter is based on the OTA-C structure, in which the central frequency of the filter is tuned by adjusting the bias voltage. The tunability of the proposed filter makes it possible to be used in eliminating power-line noise with a frequency of 50 or 60 Hz. The power consumption of the proposed filter is 13.1 nW. The total capacitance in the sixth-order band-stop filter is 54 pF, which makes it possible to integrate the proposed filter. As such, no off-chip capacitors will be needed.

CREDIT AUTHORSHIP CONTRIBUTION STATEMENT

Amirreza Solaymanpour: Formal analysis, Resources, Software, Roles/Writing - original draft. Shahbaz Reyhani: Methodology, Supervision, Validation, Writing - review & editing.

Table 4: The comparison of the proposed filter with the reported works.

	This article	[12]	[14]	[15]
Technology (nm)	180	180	250	90
Amplifier type	Folded Cascade OTA	Gm- C	Cascaded	ОТА-С
Voltage (V)	1.8	0.5	±0.8	±0.6
Number of amplifires	9	10	9	16
Cut-off frequency (Hz)	50	50	50	50
Attenuation (dB)	-102	-75	-43	-44
Capacitive capacity (nF)	0.054	0.1	0.032	0.02688
Power consumption (µW)	0.0131	280	25	0.0145

DECLARATION OF COMPETING INTEREST

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper. The ethical issues; including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, redundancy has been completely observed by the authors.

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BIOGRAPHY



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