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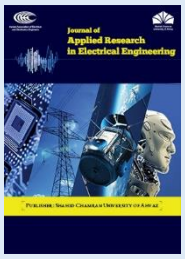

Research Article

A Fourth-order MASH DDSM for Accurate Fractional Frequency Synthesizers

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Abstract: The output of a Digital Delta-Sigma Modulator (DDSM) is always a periodic signal and the input is constant. A hybrid DDSM is a premiere to its conventional counterpart for having a potential speed, by the choice of its smaller bus. This paper offers an implementation for multi-stage noise shaping (MASH) DDSMs that includes four modulators named hybrid DDSM-1, DDSM-2, DDSM-3, and DDSM-4. Also, it introduces a new solution, where the desired ratio in fractional frequency synthesizers is formed by combining four different modulos. The first stage modulator is a programmable modulus EFM1 and has a modulus M_1 that is not a power of 2. The second, third, and fourth stage modulators are modified MASH 1-1, multi-modulus MASH 1-1-1, and the efficiently dithered MASH 1-1-1-1 modulator that have conventional modulus M_2, M_3, and M_4, respectively. The M_1 modulus is optimally selected to synthesize the new structure of the desired frequencies. Design results confirm the suppositional predictions. In addition, the results of the circuit implementation proposed method offer a 17% reduction in hardware complexity.

Keywords: Fractional frequency synthesizers, digital delta sigma modulator, dither, low complexity, hybrid modulators.

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1. INTRODUCTION

In a ΔΣ fractional-N frequency synthesizer, the multiple modulus divider is modulated by the output sequence of a digital sigma-delta modulator. Fractional-N frequency synthesis provides agile switching in narrow channel spacing systems and alleviates Phase-Locked Loop (PLL) design constraints for phase noise and reference spur. The PLL-based frequency synthesis technique is extensively employed in electronic measurement instruments, wireless communications, and class D amplifiers. The inherent problem of the fractional-N frequency synthesizer is that the periodic operation of the dual modulus divider produces fractional tones. Modern frequency synthesizers for portable applications use an indirect method known as a PLL (Fig. 1). These synthesizers consist of a Phase Detector (PD), a Loop Filter (LPF), a Voltage Controlled Oscillator (VCO), and a Multi Modulus Controller (MMC). The PC compares its two input signals phases and generates a measure of their phase error. A Low Pass Filter (LPF) must filter the phase error. The LPF takes out the DC part of the phase error. The loop is locked if the phase error is constant over time. In this synthesizer, the average output frequency is defined by:

$$f_{VCO} = \left(N_0 + \frac{N_1}{M_1}\right) . f_{PD} \quad (1)$$

where f_{PD} is the input frequency at the input to the phase detector and N_0, N_1, and M_1 are integer divider number, the input of DDSM, and modulus quantizer, respectively. Usually, the modulus M is a multiple of two.

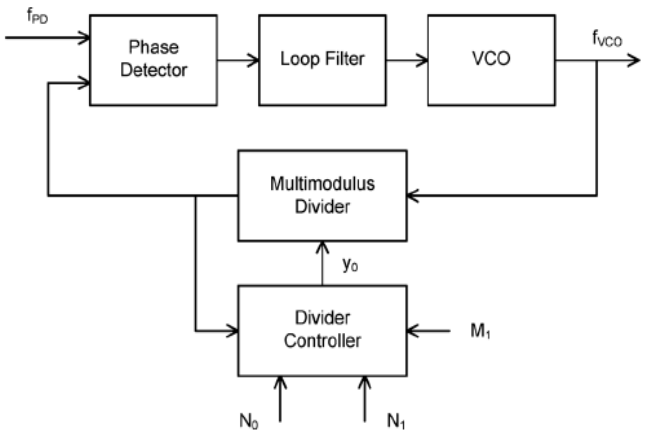

Fig. 1: Block diagram of a PLL-based fractional-N frequency synthesizer.

Input frequency multiples are synthesized by frequency synthesizers and produce higher reference frequencies and have higher frequency resolution. Since the phase detector frequency is higher than the frequency resolution in fractional-N frequency synthesizer, the loop bandwidth of the PLL is not limited by the frequency resolution. Fractional-N frequency synthesis is not useful in practical applications unless the fractional spurs are suppressed [1].

The sequence length of the output cycle is determined by the input, initial states, and DDSM architecture. There exist two classes of techniques to maximize cycle lengths in DDSMs: stochastic and deterministic. The application of additive least significant bit (LSB) dithering [2-5] is the most common stochastic technique. It can be presented at different points of the DDSM architecture to separate alternative cycles. A high-resolution digital MASH modulator can be employed to diminish the spur tone magnitude. As demonstrated by Kozak and Kale [6], the DDSM does not show large spurs with the constant input and the odd initial state of the first stage. In [7], a digital sigma delta modulator of separate lines is designed by pipeline method and its power spectral density is plotted. This method increases the speed of the modulator and reduces the hardware consumption. In [8], a ring-oscillator (RO)-based low-jitter digital fractional-N frequency synthesizer is presented. In [9, 10], the authors presented deterministic modifications to the DDSM architecture (an additional output feedback path and prime modulus) that maximize the cycle length of the error signal. Nevertheless, to have a maximal period by the modified MASH modulators, every EFM needs an extra M bit adder. Wang *et al.* [11] recommended a method for avoiding the development of spurs by substituting the sigma-delta modulator for a new type of digital quantizer and a charge pump offset incorporated with a sampled loop filter. In [12-14], a solution is presented based on mixed-radix algebra, where the required ratio is formed by combining two and three different modulus. Using error masking methodology, this modulator can decrease the hardware consumption and increase the accuracy of the fractional frequency synthesizer. In [15-17], a novel method is proposed for applying periodic dither to a DDSM to obtain minimized spurious tones. The effects of adding the pseudorandom dither signal in different stages within the proposed multi-Stage noise Shaping (MASH) modulator are expressed in a set of equations. In [18], the design of a new architecture of Continuous-Time (CT) MASH 2-2 (multi-stage noise shaping modulators) full feedforward Sigma Delta (ΣΔ) modulator is presented. In [19], it is shown that applying a linear feedback shift register (LFSR) dither to a digital delta-sigma modulator (DDSM) cannot always increase its fundamental period.

Gonzalez-Diaz *et al.* [20] proposed a technique for the dithered MASH 1-1-1 DDSM. In their structure, a dither signal is injected simultaneously at the inputs of the second and third stages of a MASH 1-1-1 DDSM. These authors suggest that an m-bit LFSR dither generator is particularly "efficient" to eliminate fractional tones. In the present work, we introduce hybrid DDSM 1-2-3-4 modulator architecture. In this method, the First Order Error Feedback Modulator (EFM1) in the first stage has a variable programmable modulus M_1 that is not a power of 2. The modulators in the second, third and four stages (M_2, M_3, and M_4, respectively) are the power of 2. This method uses separate line technology [21, 22].

In [23], the modulator was presented for the third time. In addition, the proposed modulator simulation at the transistor level has been investigated and performed. Noise level simulations and power consumption of transistors for different levels of transistors are also provided. In this paper, the structure of each stage of the modulator is designed to reduce the noise level of the output. In this paper, a 4th order modulator with a multi-stage structure is presented.

The remainder of this paper is structured as follows: Section 2 describes the MASH modulators and summarizes background. Section 3 represents the 1-2-3-4 modulator. Word length optimization is analyzed in Section 4. Section 5 illustrates the simulation results. Finally, conclusions are made in Section 6.

2. BACKGROUND

The initial block diagram of a multi-tier MASH modulator is made from a digital storage. The warehousing model is shown in Fig. 2. In this form, the input of the storage is the digital word x [n] with a length of n_0 bits. In decimal frequency synthesizers, the input is constant and sets the desired fraction value of $\frac{X}{2^{n_0}}$. The string stability of the error e [n] is delayed by one unit of time. The delay string s[n] is summed with the input signal $x[n]$. Whenever the warehouse keeper is overloaded, the transport bit $c[n]$ becomes one. The average time of the output string has a number of zeros and ones, which is equal to the average time of the input. Fig. 2b shows the digital storage model. The output string $y[n]$ corresponds to the output digit $c[n]$. If the signal $v[n]$, which is equal to the sum of the signals $x[n]$, s[n], is greater than or equal to $M = 2^{n_0}$, it overflows and $y[n] = 1$. Otherwise, it is zero. So mathematically we have:

$$c[n] = y[n] = Q(v[n]) = \begin{cases} 0, & v[n] < M \\ 1, & v[n] \geq M \end{cases} \quad (2)$$

The difference between $v[n]$ and $My\,[n]$ is fed to the input through the register, if $y[n] = 0$ then $e[n] = v[n]$ and if $y[n] = 1$ then $e[n] = v[n]$-M. Hence, we have:

$$e[n] = v[n] \mod M \quad (3)$$

This structure is called EFM, because the error signal s [n] is fed back to the storage input. Fig. 3 shows the block diagram of the digital Sigma Delta MASH modulator of the *l*st order, which consists of a cascading connection of $EFM1_N$ bit blocks and a noise cancelling network. In this negative structure, the quantization error of each stage is entered to the next stage and the output of each stage is entered into the noise removal network, which will eliminate the quantization error of the middle stages. The output of the 1st order MASH modulator in the z domain is expressed by the following equation.

$$Y(z) = \frac{1}{2^N}.X(z) + \frac{1}{2^N}(1 - z^{-1})^l.E_l(z) \quad (4)$$

The structure of the HK-EFM1 (Hosseini and Kennedy EFM) used in the HK-MASH (Hosseini and Kennedy MASH) is illustrated in Fig. 4. There is just one difference between this structure and the classical EFM1 in Fig. 2; i.e.,

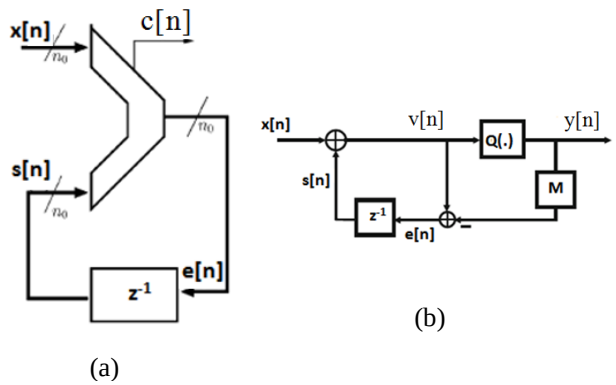

Fig. 2: (a) The digital storage used in the MASH structure, and (b) Its model

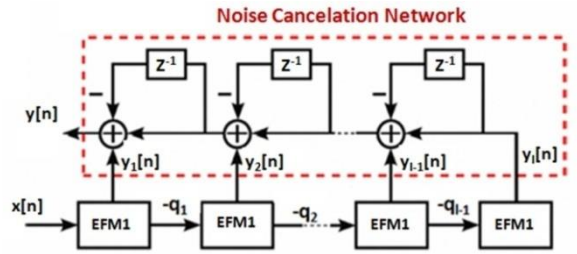

Fig. 3: Block diagram of an l^{th} order MASH DDSM incorporating a cascade of EFM1s [1].

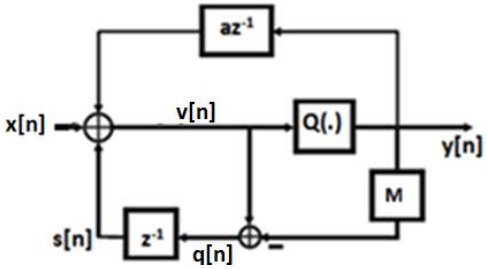

Fig. 4: The modified EFM1 used in HK-MASH [9].

the existence of the feedback block az^{-1}. Here, a is a selected small integer to make $(M-a)$ the maximum prime number below M. The cycle length of it is $(M-a)^l = (2^N - a)^l$, where l is the order of the modulator. Song and Park [24] proposed the modified MASH 1-1-1, as shown in Fig. 5. The modified MASH structure cascades several first-order digital accumulators like the traditional MASH structure but has a supernumerary feedforward connection between two adjoining categories and increases the sequence period of quantization error. The sequence period in the l^{th} MASH DDSM structure is $N_1.M^{l-1}$, where N_1 is the period of the first stage, and l is the order of the MASH modulator.

Gonzalez-Diaz *et al.* [20] added LSB dither to the second and third stages of a MASH 1–1–1, as shown in Fig. 6. Thus, the output spectrum appears to approach the ideal spectrum.

Le and Chen [25] presents a self-adaptive Sigma-Delta modulator, which offers opportunity to simplify the process of tuning parameters and further improve the noise performance. This paper presents a 5th order Sigma-Delta modulator to obtain higher SNR. Specifically, an additional 3rd order digital loop integrator is inserted between the AFE and the quantizer, which increases overall loop order to

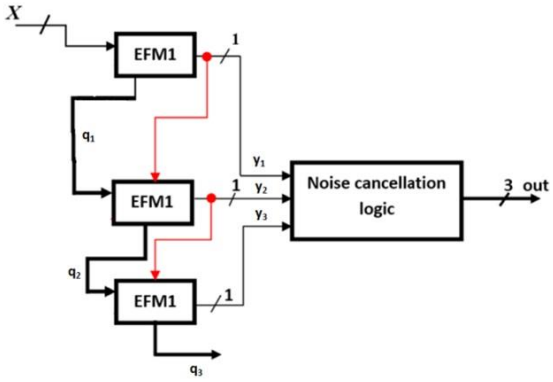

Fig. 5: Block diagram of the modified MASH 1-1-1 proposed in Sond and Park [24].

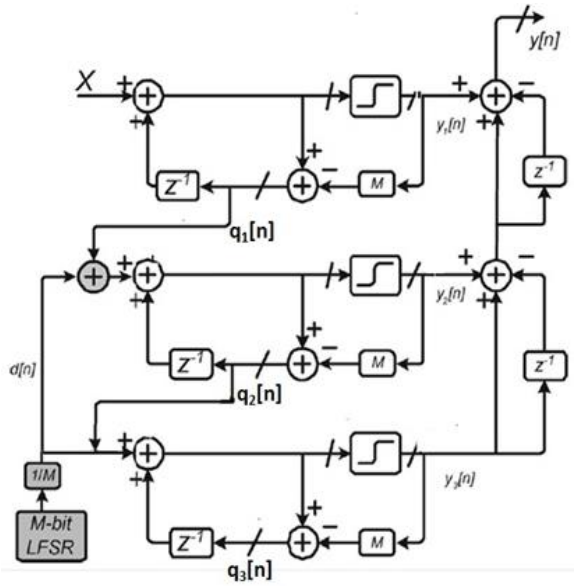

Fig. 6: Solution proposed by Gonzalez-Diaz et al. [20] for efficiently dithering a MASH 1-1-1.

produce much higher SNR for Sigma-Delta modulator and the parameters of the 3rd order digital loop integrator are optimized by swarm intelligent algorithm.

Mazzaro and Kennedy [26] presents a Fractional-N Charge Pump (CP) PLL with a Multi-stage noise Shaping (MASH) 1-1-1 divider controller to exhibit pairs of spurious tones called “horn spurs”. The phenomenon has been confirmed in measurements on a commercial wideband synthesizer.

Mai and Kennedy [27] describes a detailed analysis of the cause of wandering spur patterns in a MASH 1-1-1 DDSM-based fractional-N frequency synthesizer, supported by experimental measurements.

As shown in Fig. 1, this classical MASH 1-1-1 can be used in the fractional frequency synthesizer. In this synthesizer architecture, both f_{out} and f_{ref} are integer multiples of f_s, where $f_s = \frac{f_{ref}}{M}$ is the channel spacing. If modulus M is a power of 2, then only integer multiples f_{ref} of divided by a power of 2 can be synthesized.

The Global System for Mobile communication (GSM) system is a time and frequency division system in which a carrier frequency and a time slot number characterize each physical channel. GSM system frequencies include two bands at 900 MHz and 1800 MHz commonly referred to as the GSM-900 and DCS-1800 systems, respectively. For the primary band in the GSM-900 system, 124 radio carriers have been defined and assigned in two sub-bands of 25 MHz, each in the 890–915 MHz and 935–960 MHz ranges with the channel widths of 200 kHz.

Thus, in GSM 450, the problem of synthesizing is considered an output frequency of 0.45 GHz from a 13 MHz reference clock. In this example, $f_{ref} = 13\ MHz, f_s = 200\ KHz, f_{out} = 0.45\ GHz$ yielding, $N_0 = 34$, and $N_1 = 20648881, M = 2^{25}$. In conventional MASH 1-1-1 based fractional frequency synthesizers having $M = 2^{25}$, the required division number can be approximated as follows:

$$f_{out} = \left(34 + \frac{20648881}{2^{25}}\right).\mathrm{f_{ref}} = 0.4499999999\mathrm{GHz} \qquad (5)$$

Hence, a frequency offset is approximately 89.408 Hz.

The approximation noise can be reduced using a larger value of modulus *M*. Also, it correlates with increasing the word length of the modulator, hardware complexity, and power consumption.

3. The Proposed Method

In this section, we introduce a novel structure for the dithered MASH DDSM 1-2-3-4 that produces a long sequence period.

This paper attempts to reduce the hardware and power consumption of the fourth-order Digital Sigma-Delta Modulator and improve the noise level. Therefore, a fourth-order sigma-delta modulator with a high bit numbers broken down into several smaller sigma-delta modulators with fewer bits. Then, the input of the fourth-order modulator is divided into four segments so that each part of it is subdivided into first, second, third, and fourth-order modulators. We call this modulator, which consists of 4 sub-sections, a hybrid modulator.

The hybrid modulator architecture is shown in Fig. 7. In this architecture, instead of a single classical power-of-two modulus sigma-delta modulator in the fractional-N frequency synthesizer, we can use four modulators. The first stage modulator is a Variable Modulus EFM1 (VM-EFM1) and has a programmable modulus M_1 that is not a power of 2.

The second modulator in the hybrid structure is modified MASH 1-1, which has conventional modulo M_2. The cycle length in modified MASH 1-1 structure is ${M_2}^2$, where $M_2$is thequantizer modulus in the classical DDSM.

The third modulator in the hybrid structure is multi-modulus MASH 1-1-1, which has conventional modulo M_3. The small positive integer a in the i^{th} stage of HK EFM1 is denoted as a_i. This value will be assumed different for each stage. The values of a_i are selected such that to make $\{M - a_1, M - a_2, \dots, M - a_l\}$ co-prime numbers to maximize the period. A few values of a_i are given in Table 1.

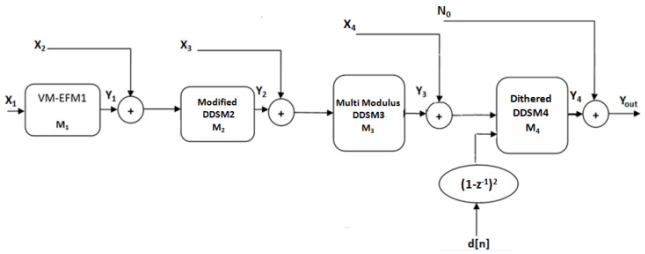

Fig. 7: Block diagram of the hybrid modulator DDSM 1-2-3-4 used in fractional frequency synthesizer.

Table 1: Some values of a_i in HK-MASH 1-1-1.

Word length (N)	a_1	a_2	a_3
4, 6, 9, 10, 12	3	0	1
3, 5, 7	1	0	3
8	5	0	1
11	9	0	1

It is of note that to make the period independent of the input, $M - a_1$ is set as a prime number.

If the greatest common divisor of any two numbers is 1, they are co-prime numbers. A prime number is a natural number that is divisible only by itself and1.

The fourth modulator in the hybrid proposed structure is dithered MASH 1-1-1-1, which a periodic LFSR dither input with a period N_d added to the third and fourth stages of MASH 1-1-1-1. Fig. 8 presents an implementation of the second-order dither hybrid modulator.

The output frequency (f_{out}) in the fractional frequency synthesizer is determined by:

$$f_{out} = (N_0 + \frac{X_4 + \frac{X_3 + \frac{X_2 + \frac{X_1}{M_1}}{M_2}}{M_3}}{M_4}).f_{ref} \qquad (6)$$

In this case, the z-transforms y_1, y_2, y_3, y_4, and y_{out} are shown by:

$$Y_{out}(z) = N_0 + Y_4(z) \qquad (7)$$

$$Y_4(z) = STF_4(z)(X_4 + Y_3(z)) + NTF_4(z)Q_4(z) \qquad (8)$$

$$Y_3(z) = STF_3(z)(X_3 + Y_2(z)) + NTF_3(z)Q_3(z) \qquad (9)$$

$$Y_2(z) = STF_2(z)(X_2 + Y_1(z)) + NTF_2(z)Q_2(z) \qquad (10)$$

$$Y_1(z) = STF_1(z).X_1 + NTF_1(z)Q_1(z) \qquad (11)$$

where STF_1, STF_2, STF_3, STF_4, NTF_1 ,NTF_2, NTF_3, *and* NTF_4 are the signal and error transfer functions of first, second, third and fourth stage modulators, respectively, and $Q_1(z), Q_2(z), Q_3(z), and\ Q_4(z)$ are the quantization error signals introduced by the first, second, third, and fourth sigma-delta modulators, respectively. X_1, X_2, X_3, and X_4 are the integer inputs of the VM-EFM1, modified MASH 1-1, multi-modulus MASH 1-1-1, and second-order dithered MASH 1-1-1-1 in the hybrid architecture, respectively. Hence, the final output y_{out} can be attained by:

$$Y_{out}(z) = N_0 + STF_4(z).X_4 + STF_4(z).STF_3(z).X_3 + STF_4(z).STF_3(z).STF_2(z).X_2 + STF_4(z).STF_3(z).STF_2(z).STF_1(z).X_1 + NTF_4(z)Q_4(z) + STF_4(z).NTF_3(z).Q_3(z) + STF_4(z).STF_3(z).NTF_2(z).Q_2(z) + STF_4(z).STF_3(z).STF_2(z).NTF_1(z).Q_1(z) \qquad (12)$$

where,

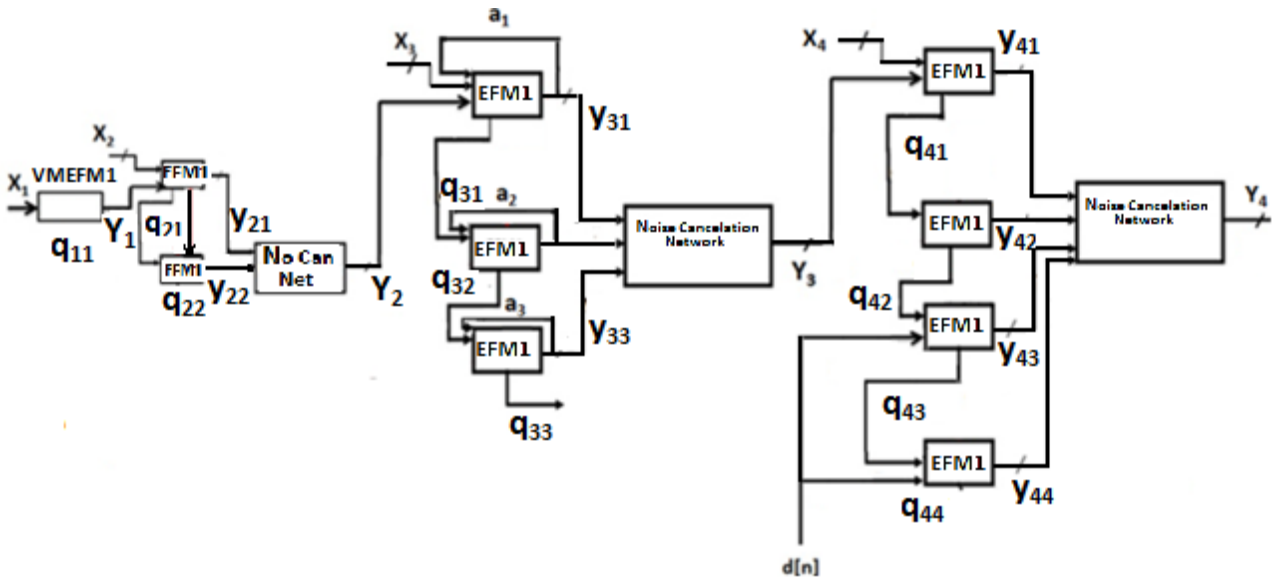

Fig. 8: Implementation of the second order dither hybrid DDSM 1-2-3-4 modulator.

$STF_4(z) = \frac{1}{M_4}, STF_3(z) = \frac{1}{M_3}, STF_2(z) = \frac{1}{M_2}, STF_1(z) = \frac{1}{M_1}, NTF_4(z) = (1-z^{-1})^4, NTF_3(z) = (1-z^{-1})^3, NTF_2(z) = (1-z^{-1})^2$, and $NTF_1(z) = (1-z^{-1})$.

4. The Design Approach

The DDSM quantization error power is distributed over a few tones that are specified by the period, leading to a tone spacing of $df[k] = \frac{f_s}{N}$, where f_s is the sampling frequency and N is the period. When the sequence length and, consequently, the number of tones is large, the Power Spectral Density (PSD) approaches the classical white noise approximation. It is noteworthy that all quantization error terms can be considered as independent additive white sources. The PSD of Y_2, Y_3, and Y_4 in the second-order LSB LFSR dither signal in the DDSM2, the multi-modulus DDSM3, and dithered DDSM4 are defined by:

$$P_2(\Omega[k]) = \frac{1}{12}(|1-z^{-1}|)^4 \Big|_{z=e^{j\Omega}} = \frac{1}{12}\left(2\sin\left(\frac{\Omega}{2}\right)\right)^4 \quad (13)$$

$$P_3(\Omega[k]) = \frac{1}{12}(|1-z^{-1}|)^6 \Big|_{z=e^{j\Omega}} = \frac{1}{12}\left(2\sin\left(\frac{\Omega}{2}\right)\right)^6 \quad (14)$$

$$\Omega[k] = \frac{2\pi}{N}.k, \quad k = 0,1,\dots,\frac{N}{2} \quad (15)$$

$$P_4(\Omega[k]) = \frac{1}{12}(|1-z^{-1}|)^8 + \frac{1}{12}\frac{1}{M_4{}^2}(|1-z^{-1}|)^4 \Big|_{z=e^{j\Omega}} \quad (16)$$

where Ω is the angular frequency of the oscillation and P is the density of the power spectrum. Also, at the output of the proposed hybrid modulator, since P_2 and P_3 are second-order and third-order shaped, respectively, while P_4 is fourth-order shaped, if the level of the lowest frequency tone in P_2 and P_3 is below that of P_4, the overall power of P_2 and P_3 should always be below the P_4 envelope. This can be expressed as:

$$P_2 < P_4, f = \frac{f_s.k}{N_2}, k = 1,2,\dots,\frac{N_2}{2} \quad (17)$$

$$P_3 < P_4, f = \frac{f_s.k}{N_3}, k = 1,2,\dots,\frac{N_3}{2} \quad (18)$$

Note that for a DDSM with an output period of N, the lowest frequency tone is at $\frac{f_s}{N}$. Therefore, since the periods for modified DDSM2 and multi-modulus DDSM3 are approximately $M_2{}^2$ and $(M_3-\alpha)^3$, respectively, the lowest frequency tones in the power spectra are at $\frac{f_s}{M_2{}^2}$ and $\frac{f_s}{(M_3-\alpha)^3}$.

Thus, at low frequencies:

$$|1-z^{-1}|^2 = \left|1-e^{\frac{-j2\pi f}{f_s}}\right|^2 = |2\sin\left(\frac{\pi f}{f_s}\right)|^2, \sin\left(\frac{\pi f}{f_s}\right) \approx \frac{\pi f}{f_s} for\ f \ll f_s \quad (19)$$

We can approximate P_2, P_3, and P_4 at low frequencies by:

$$P_2 = \frac{1}{12}\left(\frac{1}{M_3.M_4}\right)^2 2^4.(\frac{\pi f}{f_s})^4 \quad (20)$$

$$P_3 = \frac{1}{12}\frac{1}{M_4{}^2}2^6.(\frac{\pi f}{f_s})^6 \quad (21)$$

$$P_4 = \frac{1}{12}2^8.(\frac{\pi f}{f_s})^8 + \frac{1}{12}\frac{1}{M_4{}^2}2^4.(\frac{\pi f}{f_s})^4 \quad (22)$$

Substituting (20)-(22) into the constraints (17) and (18), we have:

$$\frac{1}{12}2^8.(\frac{\pi f}{f_s})^8 + \frac{1}{12}\frac{1}{M_4{}^2}2^4.(\frac{\pi f}{f_s})^4 \approx \frac{1}{12}2^8(\frac{\pi f}{f_s})^8 \quad (23)$$

$$\left(\frac{1}{M_3.M_4}\right)^2 2^4.(\frac{\pi f}{f_s})^4 < 2^8.(\frac{\pi f}{f_s})^8, f = \frac{f_s}{{M_2}^2} \quad (24)$$

$$2^6.\frac{1}{{M_4}^2}(\frac{\pi f}{f_s})^6 < 2^8.(\frac{\pi f}{f_s})^8, f = \frac{f_s}{(M_3-\alpha)^3} \quad (25)$$

Therefore:

$$\left(\frac{1}{M_4}\right)^2 < \frac{2^2.\pi^2}{{M_3}^6} \quad (26)$$

$$\begin{aligned} {M_3}^3 < 2\pi.M_4 \rightarrow 2^{3n_3} &< 2\pi.2^{n_4} \rightarrow 3n_3 \\ &< log_2(2\pi) + n_4 \rightarrow n_3 \\ &< \frac{2.65 + n_4}{3} \end{aligned} \quad (27)$$

$$\left(\frac{1}{M_3.M_4}\right)^2 < \frac{2^4.\pi^4}{{M_2}^4} \quad (28)$$

$$M_2 < \frac{\sqrt{M_3.M_4}}{2\pi} \quad (29)$$

In the VM-EFM1 accumulator, the output Y_1 will be periodic with a cycle length between two and M_1. In the worst case, the quantization noise power of VM-EFM1 is spread over (M_1-1) tones. The power in the lowest tone, after passing through MASH 1-1, multi-modulus MASH 1-1-1, and dithered MASH 1-1-1-1, is obtained by:

$$\begin{aligned} P_{tone} &= (\frac{1}{M_1.M_2.M_3.M_4})^2 \\ &= {STF_1}^2.{STF_2}^2.{STF_3}^2.{STF_4}^2 \end{aligned} \quad (30)$$

Consequently, to mask the worst-case tone from VM-EFM1 at the output of dithered DDSM 1-1-1-1, it is required that:

$$\Omega_1[1] = \frac{2\pi}{M_1}, k = 1, N_1 = M_1 \quad (31)$$

$$\mathrm{P}_4(\Omega_1[1]) \geq N_f.P_{\mathrm{tone}} \quad (32)$$

where N_f is FFT length, which presents the frequencies at which the PSD is estimated.

Substituting (22) and (30) into the constraint (32), we obtain:

$$\begin{aligned} N_f(\frac{1}{M_1.M_2.M_3.M_4})^2 \leq \frac{1}{12}(\frac{2\pi}{M_1})^8 &\rightarrow M_1 \\ \leq \sqrt[6]{\frac{(2\pi)^8.{M_2}^2.{M_3}^2.{M_4}^2}{12N_f}} & \end{aligned} \quad (33)$$

5. Design Example

5.1. Simulation Results

Given three design parameters of the reference frequency f_{ref}, the channel spacing f_s, and the output frequency f_{out}, we need to determine nine integers of $N_0, X_1, X_2, X_3, X_4, M_1, M_2, M_3$, and M_4. First, M_4 is obtained and then M_1, M_2, and M_3 are calculated.

Selecting the variable modulus EFM1, we compute:

$$p_1 = gcd(f_{ref}, f_{out}, f_s) \quad (34)$$

$$p_2 = \frac{f_{pc}}{p_1} \quad (35)$$

where $\gcd(a, b, c)$ denotes the greatest common divisor of a, b, and c. Then, the modulus M_1 is calculated as follows:

$$M_1 = \frac{p_2}{\gcd(p_1, p_2)} \quad (36)$$

M_2 and M_3 can be obtained from and (29) and (27), respectively.

Next, the inputs N_0, X_1, X_2, X_3, and X_4 can be determined.

$$I_1 = \frac{f_{out}}{f_{ref}} \quad (37)$$

The integer division number is obtained as:

$$N_0 = floor(I_1) \quad (38)$$

where *floor* (x) returns the largest integer less than x.

$$I_4 = M_4.(I_1 - N_0) \quad (39)$$

The input of dithered MASH 1-1-1-1 modulator is determined as:

$$X_4 = floor(I_4) \quad (40)$$

The input of multi-modulus MASH 1-1-1 modulator is determined as:

$$I_3 = M_3.(I_4 - X_4) \quad (41)$$

$$X_3 = floor(I_3) \quad (42)$$

The input of modified MASH 1-1 modulator is calculated as:

$$I_2 = M_2.(I_3 - X_3) \quad (43)$$

$$X_2 = floor(I_2) \quad (44)$$

The input integer number of VM-EFM1 is obtained by choosing:

$$X_1 = M_1.(I_2 - X_2) \quad (45)$$

In GSM 450, consider the problem of synthesizing an output frequency of 0.45 GHz from a 13 MHz reference clock. In this example, $f_{ref} = 13MHz$, $f_s = 200KHz$, $f_{out} = 0.45GHz$ yielding, $N_0 = 34$, $X_4 = 630, X_3 = 2$, $X_2 = 7$, $X_1 = 5, M_1 = 13, M_2 = 2^4, M_3 = 2^4$, and $M_4 = 2^{10}$. In contrast, in the classical MASH 1-1-1-1, no approximation is implicated in the hybrid modulator. In particular,

$$f_{out} = (34 + \frac{630 + \frac{2 + \frac{7 + \frac{5}{13}}{2^4}}{2^4}}{2^{10}}).f_{ref} = 0.4500\mathrm{GHz} \quad (46)$$

In order to compare classical and hybrid modulators, we demonstrate simulation results. The initial states of the first stage registers are set to odd values to avoid short cycles. The simulated output power spectrum of the classical 25-bit MASH 1-1-1-1 DDSM is shown in Fig. 9. The simulated output PSD of the hybrid DDSM 1-2-3-4 is illustrated in Fig. 10. As expected, the hybrid DDSM 1-2-3-4 achieves an almost identical PSD compared to the traditional 25-bit MASH 1-1-1-1.

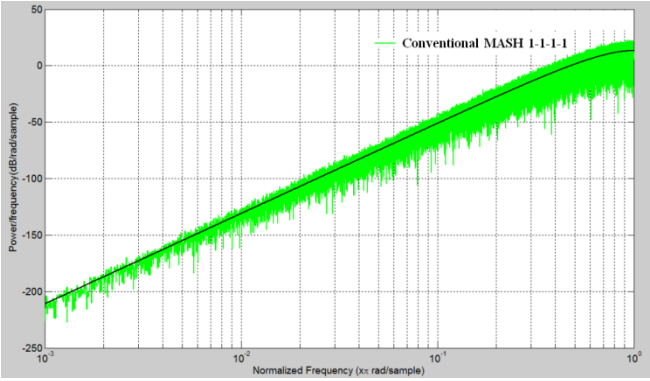

Fig. 9: Simulated PSD at the output of a second-order dithered classical MASH 1-1-1-1 DDSM; the input is 20648881, $M = 2^{25}$. The solid black curve shows the PSD of the fourth-order shaped quantization noise of MASH 1-1-1-1 with second-order shaped additive LSB dither.

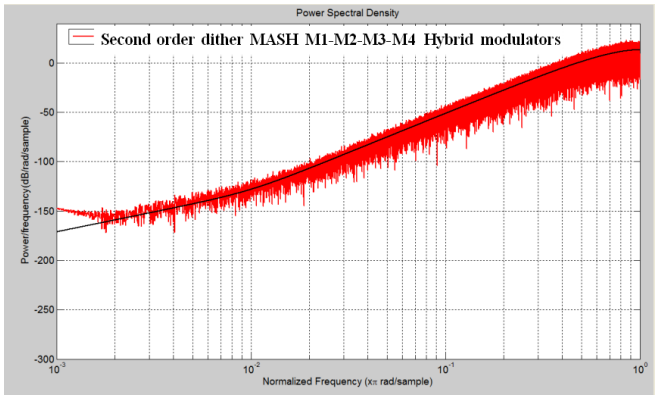

Fig. 10: Simulated PSD at the output of a second-order dithered hybrid DDSM 1-2-3-4; the inputs are $X_4 = 630, X_3 = 2,\ X_2 = 7, X_1 = 5$, the modulus are $M_1 = 13$, $M_2 = 2^4, M_3 = 2^4$, and $M_4 = 2^{10}$. The FFT length is $N_f = 2^{18}$. The solid curves assume shaped white quantization noise including second-order shaped additive LSB dither.

5.2 Hardware Complexity

The first stage of the hybrid modulator consists of an accumulator with variable module $M_1 = 13$, which is not a multiple of 2 and has the input of $X_1 = 1$. The digital implementation of this feedback modulator with the variable module is shown in Fig. 11. The signal is X_1 input and M_1 modulo. The modulator consists of a subtractor, a multiplexer, and a NOT gate. This modulator is more complex than the fixed multiplier 2 modulators, which include the adder and the register [16].

The output of VM-EFM1 can be represented as:

$$y = \begin{cases} 0, & v < \mathrm{M}_1 \\ 1, & v \geq \mathrm{M}_1 \end{cases} \tag{47}$$

The error feedback signal in this modulator can be obtained as follows:

$$e[n] = v - \mathrm{M}_1 . y \tag{48}$$

In case v[n] is greater than M_1, the sign bit of subtractor is 0, the output signal $y[n]$ will be 1, and the selection input

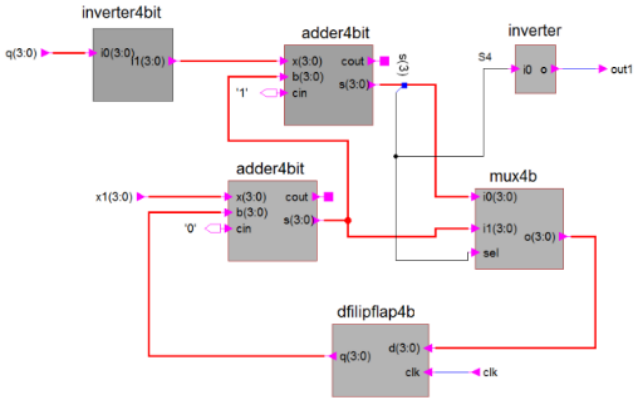

Fig. 11: Digital implementation of a First-Order VMFEM.

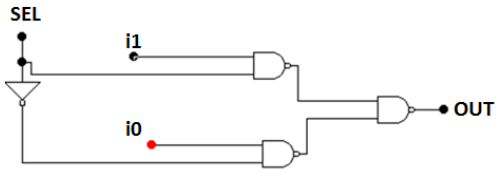

Fig. 12: The 2 × 1 multiplexer circuit.

of MUX is 0. Therefore, $e = v - M_1$. On the other hand, when $v[n]$ is smaller than M_1, the sign bit of subtractor is 1, $y[n]$ will be 0, and $e = v$.

Each 4-bit adder is made with a 1-2-1 Carry Skip Adder (CSA) structure. The 2 × 1 multiplexer circuit is shown in Fig. 12. This circuit has three NAND gates and one inverter. A 2-complement performance of the noise cancellation network needs 6 flip-flops and 18 full adders. Thus, the number of flip-flops and full-adders required to implement a conventional N-bit MASH 1-1-1-1 DDSM can be written as:

$$n_{FF} = 4N + 6, n_{FA} = 4N + 15 \tag{49}$$

Consequently, the total Hardware Consumption (HC) of the traditional N-bit MASH 1-1-1-1 DDSM is given by:

$$HC_{conv} = 8N + 21 \tag{50}$$

The number of flip-flops and full-adders required to implement the proposed hybrid DDSM 1-2-3-4 is given by:

$$n_{FF} = 4n_4 + 3n_3 + 2n_2 + n_1 + 10 \tag{51}$$

$$n_{FA} = 4n_4 + 4n_3 + 3n_2 + n_1 + 25 \tag{52}$$

Hence, the total hardware consumption of the proposed hybrid DDSM 1-2-3-4is given by:

$$HC_{Hy} = 8n_4 + 7n_3 + 5n_2 + 2n_1 + 35 \tag{53}$$

The Relative Hardware Consumption (RHC) of our hybrid DDSM 1-2-3-4 designed compared with the traditional DDSM4 is:

$$RHC\% = \frac{8n_4 + 7n_3 + 5n_2 + 2n_1 + 35}{8N + 21}\%100 \tag{54}$$

The RHC is demonstrated as the number of Look-Up Tables (LUTs), number of Flip-Flops (FFs), and the Total-Equivalent-Gate (TEG) count. In the example of Fig. 9 and Fig. 10, RHC is 83% from below for large N, suggesting that a hardware saving of at least 17% can be expected for typical values of N.

Table 2: Hardware reduction comparison.

FF & LUC	Area	Type	Ref.
98	2250 μm^2	MASH 1-1-1-1 (23 bit)	[13]
105	2050 μm^2	DDSM 4 (23 bit)	[22]
92	2150	MASH 2-2 (23 bit)	[23]
90	2100 μm^2	DDSM 4 (23 bit)	[24]
82	1750 μm^2	The DDSM 1-2-3-4 (4-4-4-10 bit)	Proposed method

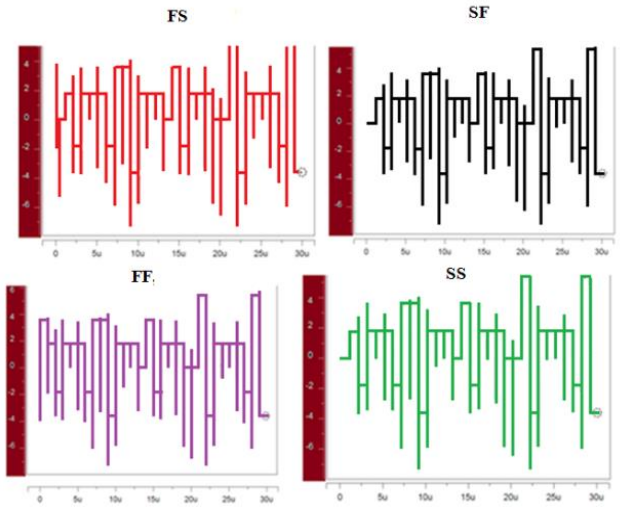

Fig. 13: The waveforms of the sigma delta modulator proposed by the 0.18 μm CMOS. The inputs are X_1 = 5, X_2 = 7, X_3 = 2, X_4 = 630 and M_1 = 13, M_2 = 16, M_3 = 16, M_2 = 2 ^{10} and f_s= 1 MHz.

These results are based on the map report from the Xilinx ISE program. In terms of overall complexity, the 4-4-4-10 bit 1-2-3-4 hybrid DDSM4 requires 17% less hardware than the conventional 25-bit MASH 1-1-1-1 DDSM and has the marginally better spectral performance.

The synthesized hardware specifications for conventional and hybrid architectures are summarized in Table 2. It is notable that the proposed circuit requires 22% of the area as the conventional solution.

The results of Monte Carlo analysis are shown in Table 3. In this table, the power dissipation of transistors in the proposed method is compared for different models of transistors. In Fig. 13, the waveform of the modulator time domain is plotted after simulating different transistor models. The figure illustrates the Temperature effects and Mismatches of transistor simulation. Fig. 14 presents the Monte Carlo simulation results of temperature, noise, and delay variations.

6. Conclusion

This paper presents a novel method for digital delta sigma modulators (DDSMs) that can be used for precision frequency synthesizers. The hybrid DDSM 1-2-3-4 has four stages and the inputs of these stages are fixed numbers. The first stage of this modulator is programmable EFM1 and the module is not power of two. The second stage is a second-order modulator whose modulus of power of 2. The third stage is a third-order modulator with different modules and the fourth stage is a fourth-order modulator with a dither signal. Optimal input signals are applied to each modulator to provide error masking. In this method, the input with high word length is divided into several optimal and smaller parts and each input is applied to a modulator. Therefore, because smaller inputs are applied to third- and fourth-order modulators, the hardware consumption is reduced by 17% and improves power consumption. It also simulates corner effects.

Table 3: Comparison of power dissipation hybrid modulator structure. The proposed modulator is 4-4-4-10 bit with different transistor models n, p.

Types of transistors in proposed hybrid modulator	Power dissipation (nW)
TT	14.06
FF	75.36
FS	71.09
SF	16.75
SS	80.12

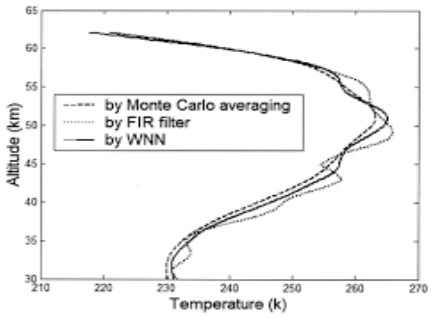

Fig. 14: The Monte Carlo design analyzing.

Credit Authorship Contribution Statement

Seyed Ali Sadatnoori: Conceptualization, Funding acquisition, Investigation, Software, Writing - review & editing.

Declaration Of Competing Interest

The author declares that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper. The ethical issues; including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, redundancy has been completely observed by the authors.

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BIOGRAPHY

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